Unit - 1

MOS Transistor Principle

MOS logic families (NMOS and CMOS), Ideal and Non-ideal IV characteristics - CMOS devices. MOS (FET) Transistor characteristics under static and dynamic conditions - Technology scaling - Power consumption.

MOS Transistor :

The MOSFET (Metal Oxide Semiconductor Field effect Transistor) is a semiconductor device which is widely used for switching and amplifying electronic signals in the electronic devices.

The MOSFET is a four terminal device with Source (S), Gate (G), Drain (D) and Substrate (B) terminals.

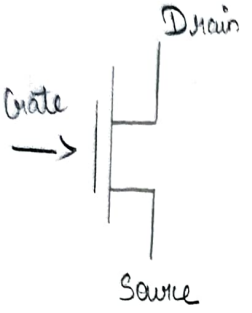
The Substrate of the MOSFET is frequently connected to the Source terminal so making it a three terminal device like field effect Transistor (FET).

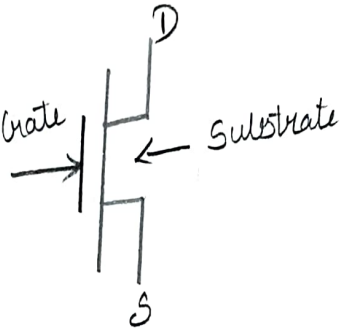
The Source (S) terminal serves as the source of the carriers of either electrons or holes.

The drain (D) terminal collects the carriers

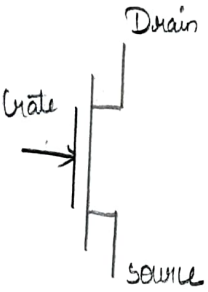
flown from the source terminal.

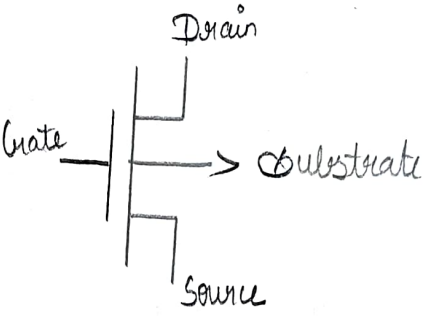
NMOS Transistor symbol :





PMOS Transistor symbol :





Depending on how the channel is created, MOSFET's are classified into two types,

a.) Enchancement type MOSFET

b.) Depletion Type MOSFET

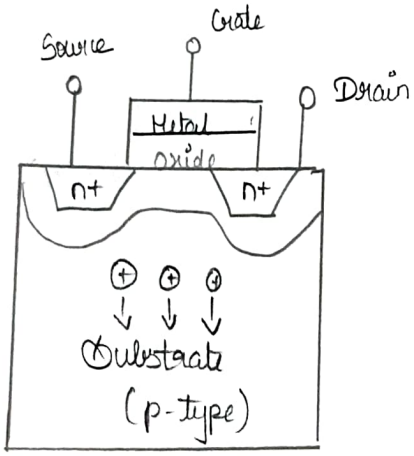
Operation of NMOS Transistor :

If a voltage is applied at the gate terminal, a conducting channel is formed underneath the oxide layer between the source and drain.

A MOSFET is called N-channel or NMOS when the channel is formed with electrons, whereas it is called as p-channel or simply PMOS when the channel is formed with holes.

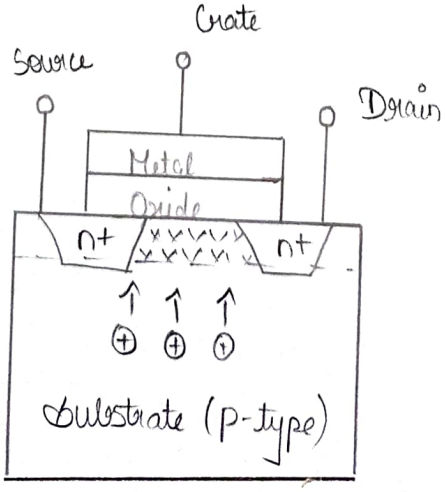
i) Body Bulk

$0 < V_{gs} < V_t$



ii) Body Bulk

$V_{GS} \geq V_t$



Depending on the voltage applied at the gate terminal, the operation of MOS is divided into three conditions.

- → Accumulation
- → Depletion
- → Inversion

Accumulation (V_{GS} is negative)

=> If a negative voltage is applied at the gate terminal, so there is a negative charge on the gate. The positively charged holes from the p-type substrate are attracted towards the gate terminal and are accumulated underneath the gate oxide layer.

=> This condition is known as accumulation.

Depletion (V_{GS} is small positive)

=> If a small positive voltage is applied, the holes will be repelled into the substrate. The repelled holes will move into the holes and create negatively charged fixed acceptor ions underneath the gate oxide layer.

=> This fixed negatively charged ions form the depletion layer.

Inversion (V_{GS} is large positive)

=> If the positive gate voltage is large enough, the holes were repelled into the substrate and the small number of free electrons in the substrate is attracted towards the gate oxide surface.

=> The attracted electrons gets accumulated underneath the gate oxide layer and forms a conducting path between the source and drain.

=> This conducting path is known as channel and the condition is known as inversion.

MOS Logic Families (NMOS & CMOS)

Complementary CMOS:

=> The most widely used logic style is static complementary CMOS.

=> The static CMOS style is really an extension of the static CMOS inverter to multiple inputs.

=> The primary advantage of the CMOS structure is robustness (i.e. low sensitivity to noise), good performance and low power consumption (with no static power consumption).

=> A static CMOS gate is a combination of two networks, called the pull-up network (PUN) and pull down network (PDN).

The NAND Gate :

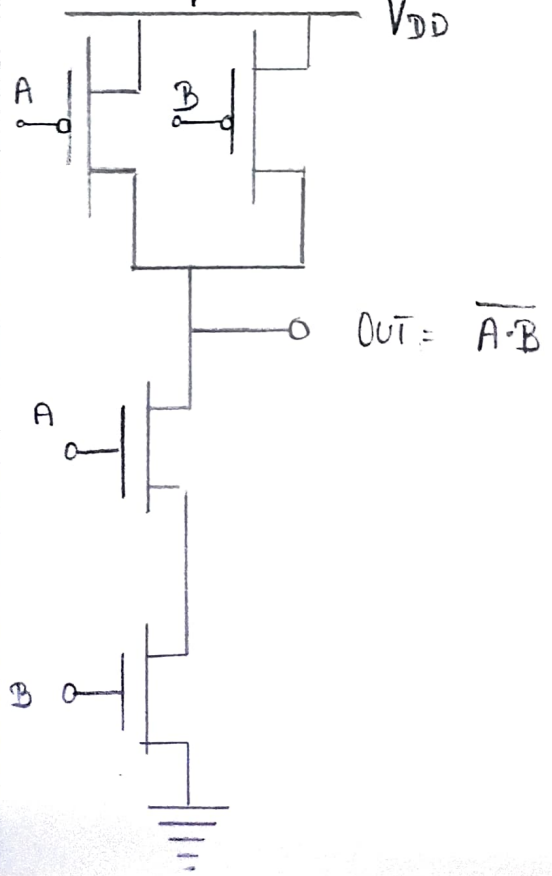
=> A two input NAND Gate ($F = \overline{A \cdot B}$)

=> The PDN network consists of two NMOS devices in series that conduct both A and B are high.

=> The PUN, the dual network consists of two parallel PMOS transistors.

=> This means that F 1 if A = 0 or B = 0 which is equivalent to $F = \overline{A \cdot B}$

Two - input Nand Gate



Truth Table

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

The NOR Gate :

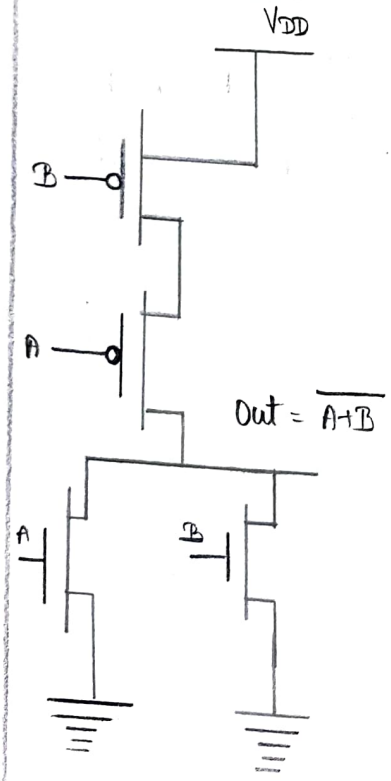
=> The two input NOR Gate ($F = \overline{A+B}$)

=> The PDN network consists of two NMOS devices in parallel that conduct when both A and B are high.

=> The PUN is the dual Network and consists of two series PMOS transistors.

=> The F is 1 if $A = B = 0$ which is equivalent to $F = \overline{A+B}$.

NOR Gate :



Truth Table

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Ideal and Non-Ideal IV characteristics :

Mos transistors have three regions of operation,

=> cutoff or subthreshold region

=> Linear or non saturated region

=> Saturation region

cutoff region :

=> There is no channel is formed between the source and the drain.

=> Almost Zero current flow.

$$I_{DS} = 0 \quad \text{when} \quad V_{GS} < V_t$$

Linear Region :

=> $V_{DS} < V_{GS} - V_t$ and $V_{GS} > V_t$ the NMOS is operating in the Linear region.

=> The potential difference between the drain and source is

=> $V_{DS} = V_{GS} - V_{GD}$

=> when a small positive potential is applied to the drain ($V_{DS} > 0$), current I_{DS} flows

through the channel from drain to source.

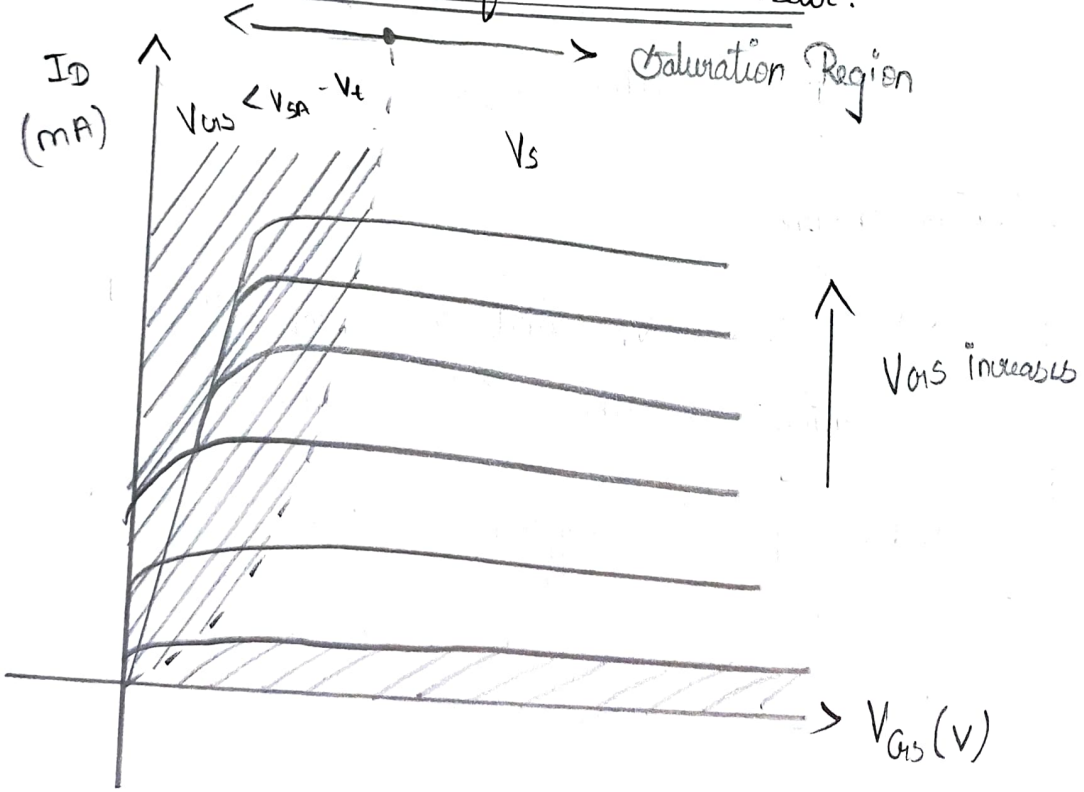
=> This mode of operation is called linear (or) resistive (or) non-saturated mode

Saturation Region :

For $V_{DS} > V_{GS} - V_t$ and $V_{GS} > V_t$ the NMOS is operating in the saturation region.

When V_{DS} is sufficiently large, then the channel is no longer inverted near the drain and become pinched off.

Ideal V-I characteristics of NMOS Transistor :



MOSFET Capacitances :

The MOSFET structure is basically a capacitative structure in which the thin gate oxide layer (dielectric) is separated by metal or polysilicon gate electrode at the top and semiconductor substrate at the bottom.

The gate Oxide capacitance is expressed as

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}.$$

It is classified into two types,

- ★ Oxide - related capacitance
- ★ Junction capacitance.

Oxide Related capacitance :

⇒ The Oxide Related capacitance are purely due to the gate Oxide structures are called gate capacitance.

⇒ There are three components of the gate capacitance with respect to the other three terminals of the MOSFET,

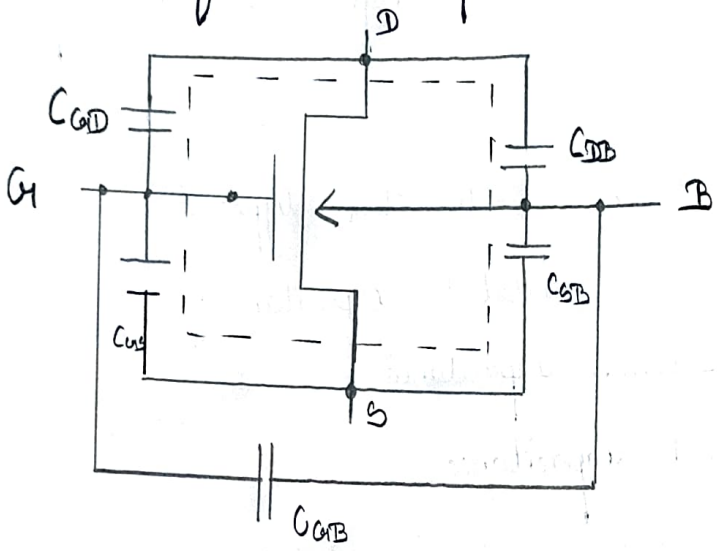
- ★ Gate to Source capacitance (C_{gs})
- ★ Gate to drain capacitance (C_{ds})
- ★ Gate to bulk capacitance (C_{bs})

$$C_{gb} = C_{ox} \times W \times L$$

$$C_{gs} = C_{gd} = \frac{1}{2} \times W \times L \times C_{ox}$$

$$C_{gs} = \frac{2}{3} WL \times C_{ox}$$

Representation of MOSFET capacitance :



$$C_{GS} = C_{gs} + C_{GSO}$$

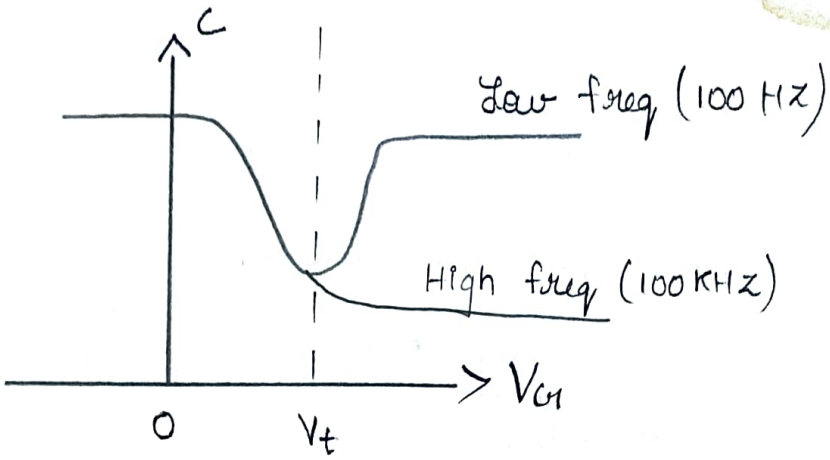
$$C_{GD} = C_{gd} + C_{GDO}$$

$$C_{GB} = C_{gs}$$

$$C_{SB} = C_{s\text{-}diff}$$

$$C_{DB} = C_{D}\text{-}diff \; .$$

MOS C-V characteristics :



Non- Ideal I-V Effects (or) Second order Effects :

Velocity Saturation and Mobility Degradation :

The saturation current I_{DS} increases less than quadratically with increasing V_{gs}. This is caused by two effects : Velocity saturation (Limiting of carrier velocity at high field) and Mobility degradation.

Velocity Saturation :

Velocity saturation : $I_{DS} = C_{ox} W (V_{gs} - V_t) V_{sat}$

Mobility Degradation :

Strong Vertical electric fields resulting from Large V_{gs} cause the carriers to scatter against the surface and also reduce the carrier mobility μ. This is called as Mobility Degradation.

Channel Length Modulation:

⇒ Increasing V_{DS} decreases the effective channel length results in higher current, thus I_{DS} increases.

⇒ When $V_{gs} < V_t$, the current drop off exponentially rather than abruptly become zero. This is called subthreshold conduction.

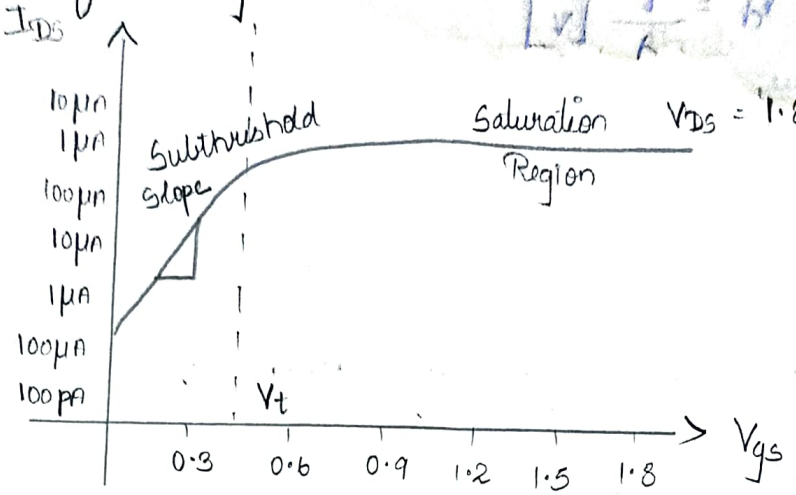
⇒ The threshold voltage itself is influences by the voltage differences between the source and body, this is called body effect.

⇒ The source and drain diffusions are reverse, biased diodes and also experiences junction leakage into the substrate well. The current into the gate I_g is ideally 0. However, as the thickness of gate oxides reduces to only a small number of atomic layers, electrons tunnel through the gate, causing some gate current.

Subthreshold Conduction:

Subthreshold conduction is exacerbated by drain induced barrier lowering (DIBL) in which a positive V_{DS} effectively reduces V_t. This effect is especially in short-channel transistors.

Source of Leakage current when transistor is off:



Threshold Voltage:

$$V_t = V_{to} + \gamma \left(\left| \sqrt{1 - 2\phi_F + V_{SB}} \right| - \sqrt{1 - 2\phi_F} \right)$$

when the parameter γ (Gamma) is called the body effect condition co-efficient, and expresses the impact of changes in V_{SB}.

Observe that the threshold voltage has a positive value for a typical NMOS device, while it is negative for normal PMOS transistor.

Early Voltage:

Accurate expression for drain current for a MOSFET in saturation is

$$I_D = K(V_{GS} - V_t)^2 \left(1 + \lambda V_{DS} \right)$$

when the value of λ is a MOSFET device parameters with unit of 1/V. Typically this value is small ranging from 0.005 to 0.02 V.

$V_A = \frac{1}{\lambda}$ [V]

Thus the drain current for a MOSFET in saturation can be expressed as

$$I_D = K(V_{GS} - V_t)^2 \left(1 + \frac{V_{DS}}{V_A}\right)$$

MOS Transistor Figure of MERIT (ω_0)

$$\omega_0 = \frac{g_m}{C_g} = \frac{\mu_n (V_{gs} - V_t)}{L^2}$$

$$= \frac{1}{\tau_n}$$

This shows that switching speed depends on gate voltage above threshold and on carrier mobility and inversely as the square of the channel length

CMOS devices - MOSFET Transfer characteristics under static & Dynamic conditions:

The operation of CMOS can be divided into five regions. They are

Region A,

the NMOS transistor is OFF and the pMOS transistor pulls the output to V_{DD}.

Region B,

the nMOS transistor is ON, the pulling the output down.

Region C,

both the transistors are in saturation. In this region $V_{in} = V_{DD}/2$ corresponding to infinite gain. Real transistors have finite output resistance.

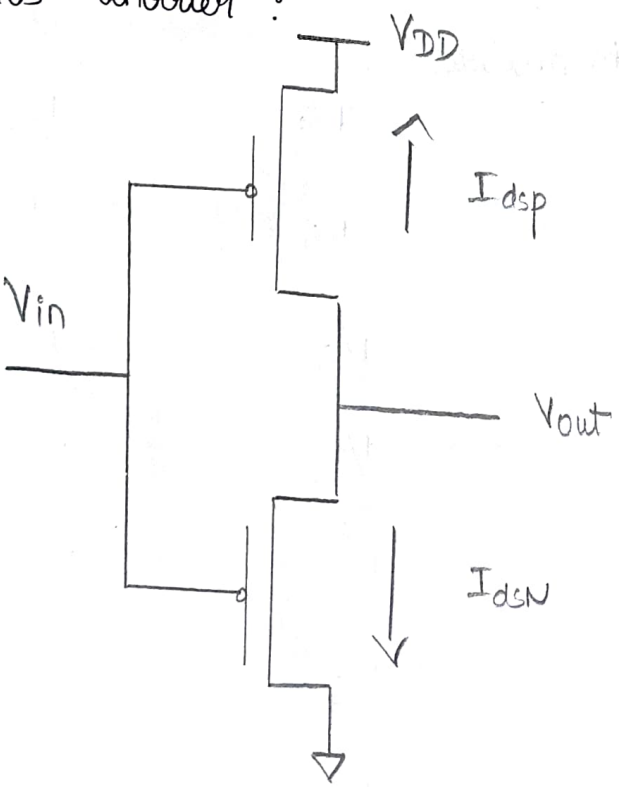
Region D,

the pMOS transistor is partially ON.

Region E,

it is completely in OFF condition, leaving the nMOS transistors to pull the output down to GND

CMOS inverter :



Technology Scaling :

Transistor scaling

constant field scaling : To the critical phenomenon are scaled by a dimensionless factor of S. these include.

- ★ All dimensions (x, y, z dimensions)
- ★ Device Voltages
- ★ Doping Concentration densities

Influence of scaling on MOS device characteristics :

Parameter	Sensitivity	Constant Voltage	Lateral
	Scaling Parameters		
Length L		1/S	1/S
Width W		1/S	1
Gate Oxide thickness t_{ox}		1/S	1
Supply Voltage : V_{DD}		1/S	1
Threshold Voltage V_{in}, V_{tp}		1/S	1
Substrate doping : N_A		1/S	1
	Device characteristics		
β	$\frac{W}{L}\frac{1}{t_{ox}}$	S	S

Current : I_d	$\beta(V_{DD} - V_t)^2$	S	S
Resistance : R	$\frac{V_{DD}}{I_{dH}}$	1/S	S
Gate capacitance	WL/t_{ox}	1	1/S
Gate delay : τ	RC	1/S	1/S
Clock frequency : f	$1/\tau$	1/S	$1/S^2$
Chip Area : A	-	S	S^2
Power density	P/A	1	S
Current density	I_{dx}/A	S	S

Constant Voltage Scaling Factor :

Feature sizes are shrink from 6 μm to 1mm while maintaining a 5V supply voltage.

Interconnect Scaling :

To common approaches to interconnect scaling are to either scale all dimensions or keep the wire height constant.

Power Consumption :

The Power dissipation in digital CMOS circuits can be described by,

$$P_{avg} = P_{dynamic} + P_{sc} + P_{Leakage} + P_{static}$$

Technology Scaling :

Transistor Scaling

Dynamic Power Dissipation :

The dynamic power dissipation, $P_{dynamic}$ is caused by the charging and discharging of capacitances in the circuit.

Short circuit Dissipation :

The short circuit power consumption $P_{short-circuit}$ is caused by the current flow through the direct path existing between the power supply and the ground during the transition phase.

The short circuit current power dissipation is expressed by

$$I_{short-circuit} = k/V_{DD} \cdot (V_{DD} - 2V_{ip})^3 \cdot \tau \cdot N \cdot f$$

$$P_{short\ circuit} = K \cdot (V_{DD} - 2V_{ip})^3 \cdot \tau \cdot N \cdot f$$

where K is a constant that depends on the transistor sizes. V_{th} is the threshold Voltages of the nMOS and PMOS.

τ is the rise or fall time of input Signal.

N is the average number of transitions.

The Leakage power dissipitation, $P_{leakage}$ is caused due to;

=> Reverse bias diode Leakage current at the transistor drains.

=> Subthreshold current through a turned off transistor channel

=> Grate induced drain Leakage

=> Grate oxide tunneling

Grate induced Drain Leakage:

* It is caused by high field effect in the drain junction of MOS Transistors.

$$I_{GIDL} = A E_S \cdot e^{-B/E_x}$$

* where E_S is the transverse electric field at the surface, thinner oxide T_{ox} and higher supply voltage Vdd increases G_{IDL}.

* G_{IDL} is also referred to as surface band to - band tunneling Leakage.

Scaling

Static Power Dissipation :

Ideally, in the steady state of CMOS circuits there is no static power dissipation and this is the most attractive characteristic of CMOS technology.

1. Define any two layout design rules
Micron design ....

UNIT-2

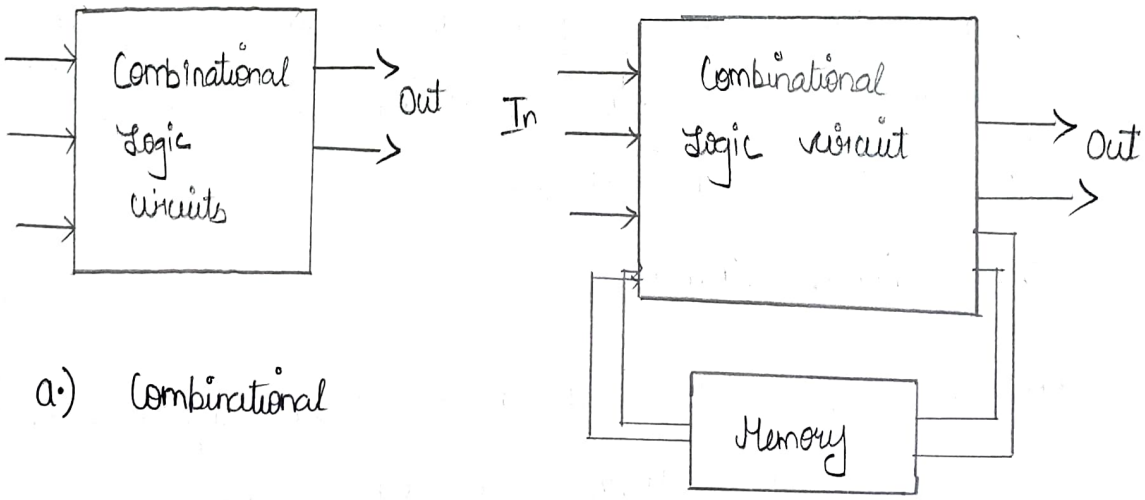
Combinational Logic Circuits

Propagation Delays, stick diagram, Layout diagram, Examples of combinational Logic design, Elmore's constant, static Logic gates, Dynamic Logic gates, Pass Transistor Logic, Power dissipation, Low-Power design principles.

Introduction :

Combinational circuits are those whose outputs depend only on the present inputs while sequential circuits have Memory.

The combinational Logic gates can be constructed by using NMOS and PMOS transistors.



a.) Combinational

b.) Sequential

Propagation Delay:

The overall propagation delay of the inverter is defined as the average of two values:

$$t_p = \frac{(t_{pHL} + t_{pLH})}{2}$$

cycle time t_{cyc} is the time between identical points of successive cycles in the signal waveform as seen at any single node. Often cycle time is specified in terms of in reciprocal, clock frequency f_{clk}.

Stick Diagrams:

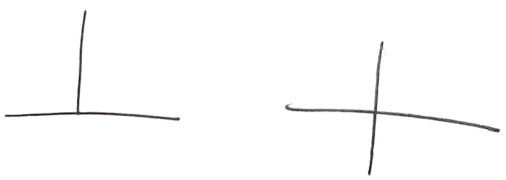
VLSI designs aim to translate circuit concepts onto silicon. Design processes are aided by simply concepts such as stick and symbolic diagrams.

Key element is a set of design rules.

Defn: A stick diagram is a simple way of representing the layout by using the thick lines with their interconnection.

Stick diagram Rules:

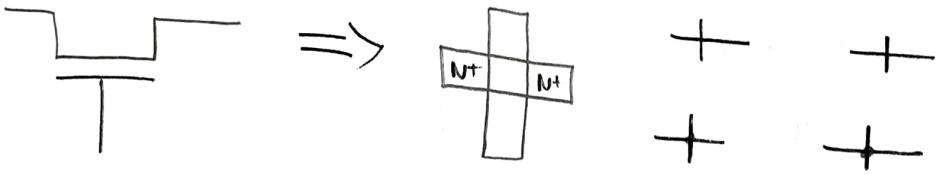
Rule: 1 when two or more 'sticks' of the same type cross or touch each other represent electrical contact.



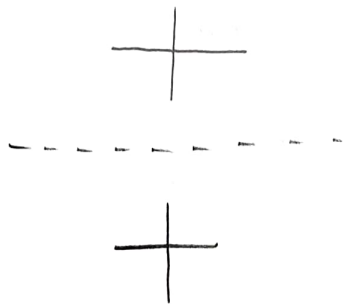
ture sizes and
solute dimen...

Rule 2: when it does not satisfy Rule 1, there is no electrical contact.

Rule:3 when a poly crosses diffusion it represents a transistor. If a contact is shown then it is not a transistor. A transistor exists where a polysilicon crosses either an N diffusion (green) stick (green) or P diffusion (yellow) stick (PMOS transistor).



Rule: 4 In CMOS a demarcation lines is drawn to avoid touching of p-diff with n-diff. All PMOS must lie on one side of the line and all NMOS will have to be on the other side.



Layout Design Rules:

MOS circuits are formed on four basic layers

=> N- diffusion
=> P- diffusion
=> Polysilicon
=> Metal

Stick Diagrams

Stick diagrams may be used to convey layer information through the use of a color code.

Eg: -> n- diffusion - green
-> Poly - red
-> blue - Metal

The three different representation are useful in different contexts:

circuit diagram - Used to plan the logic of the system.

Stick diagram - Used to plan the topology of the system layout.

Layout - final decisions of sizes.

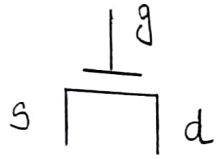
Pass Transistors :

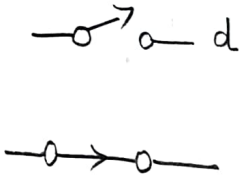
A popular widely used alternative to Complementary CMOS is pass transistors logic.

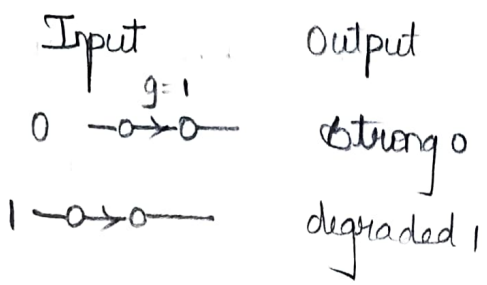
Pass transistor logic attempts to reduce the number of transistors required to implement logic by allowing the primary inputs to drive gate terminal such as source / drain terminals.

NMOS and PMOS Pass transistors :

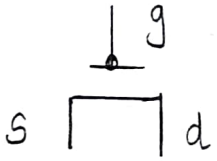
nMOS:

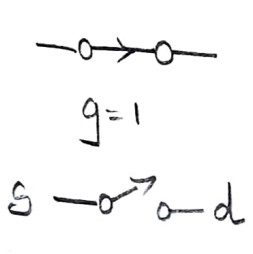


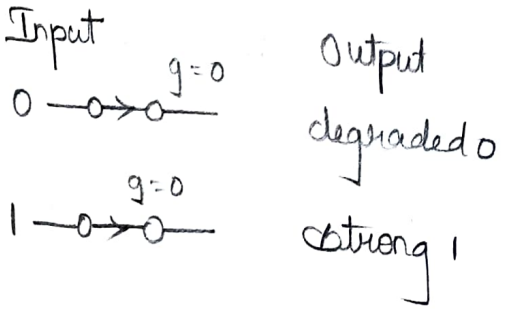




pMOS





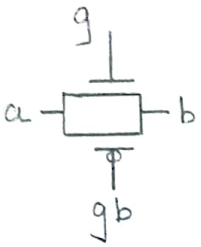


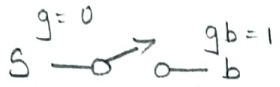
Transmission Gate :

Transmission Gates used as a Multiplexing element, a logic structure, a latch element and an Analog Switch. The most widely used solution

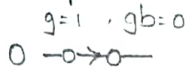
to deal with the voltage drops induced by pass transistors is the use of transmission gates.

CMOS transmission Gate :

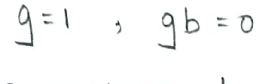


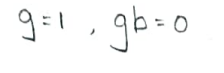


Input Output

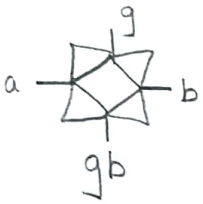


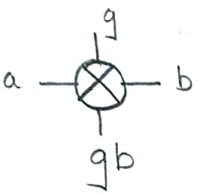
Strong 0

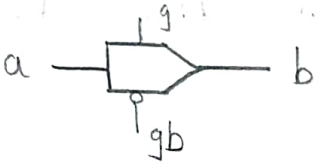




Strong 1







Low Power Design Principles :

Low Power design in terms of system, algorithms architecture, circuits and process devices has received significant attention and research input over the last decade.

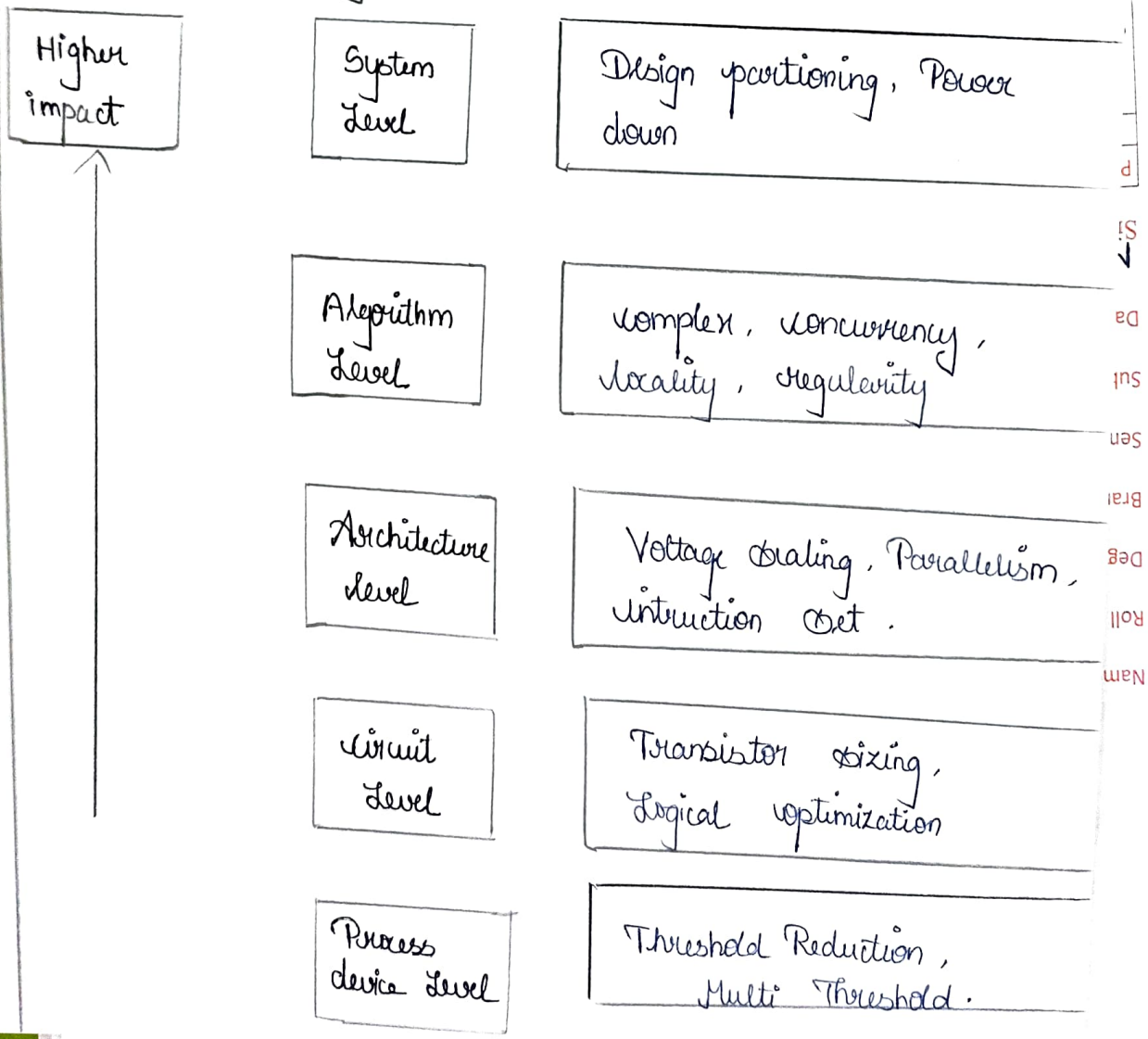
The Power dissipation is a strong function of transistors sizing input and output rise / fall time, device thresholds and temperature, switching activity.

Increasing challenges of Power:

- ★ Increasing device densities
- ★ Increasing clock frequencies
- ★ Lowering Power supply Voltages
- ★ Lowering transistor threshold Voltages

High power consumption → higher temperature → heat sinks, ceramic packaging (expensive).

Low Power design levels:



Unit - III

Sequential Logic circuits and clocking Strategies

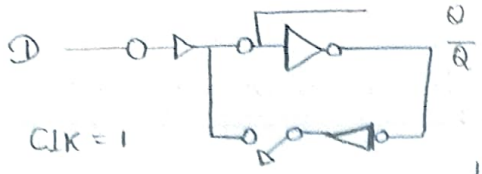
Static Latches and Registers, Dynamic latches and Registers Pipelines, Nonbistable Sequential circuits. Timing classification of digital systems, Synchronous Design, Self timed circuit design.

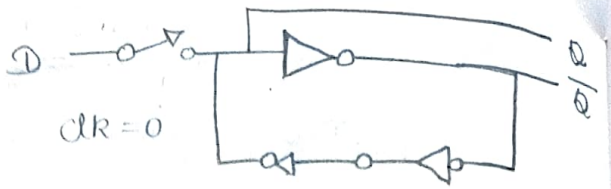
Introduction:

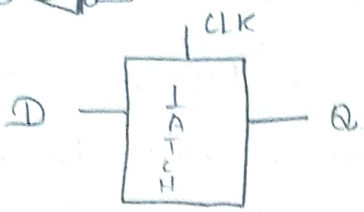
Sequential Systems consists of combinational logic and registers which hold the system state in which all registers are under the control of a single global clock, whose outputs are functions of the current inputs and current state. The next state is determined based on the current state and the current inputs.

Static Latches:

A latch is an essential component in the construction of an edge-triggered register. It is the level sensitive circuit that passes the D input to the Q output when the clock signal is high. This latch is said to be in transparent mode. when the clock is low, the input data sampled on the falling edge of the clock is held stable at the output at the entire phase, and the latch is in hold mode.







Static Registers :

* A collection of D-flip flops sharing a common clock input is called a register.

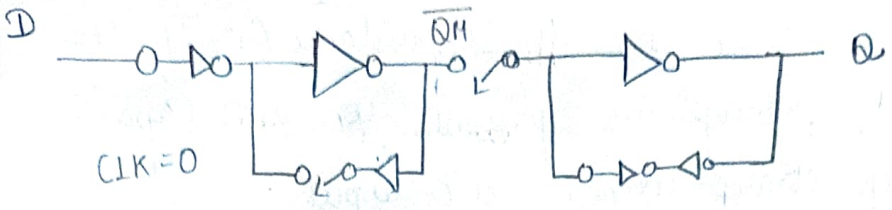
* By combining two level-sensitive latches, one negative and one sensitive and one positive negative sensitive. we construct the edge-triggered flip flop.

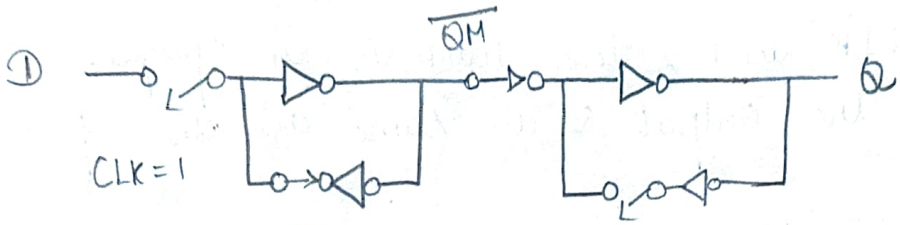
* The first latch stage is called the master and the second is called the slave.

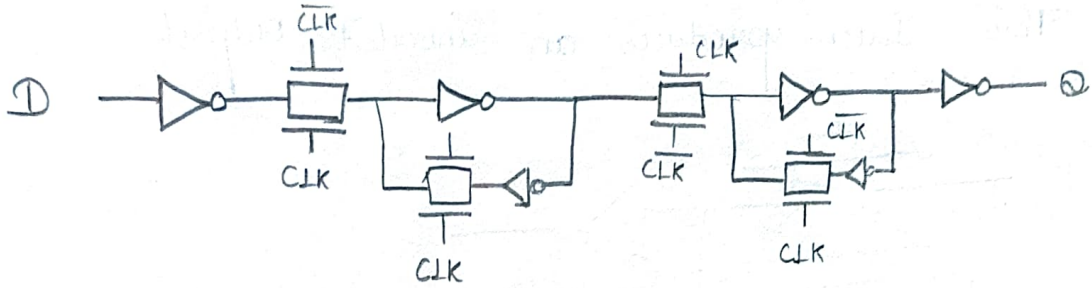
-> while CLK is low, the master negative-level sensitive latch output (QM) follows the D input while the slave positive level sensitive latch holds the previous value.

-> when the clock transition from 0 to 1, the master latch becomes opaque and holds the D value at the time of clock transition.

-> when the clock transition from 1 to 0, the slave latch holds its value and the master starts sampling.







Dynamic Latches and Registers :

That a stored value remains valid as long as the supply voltage is applied to the circuit, hence the name static

The major disadvantage of the static gate, however, is its complexity. The principal is exactly identical to the one used in dynamic logic - charge stored on a capacitor.

Dynamic latch :

* A Dynamic latch consists of transmission gate, inverter and capacitance.

* Dynamic latches are reduce transistor count, eliminate feedback inverter and transmission gate.

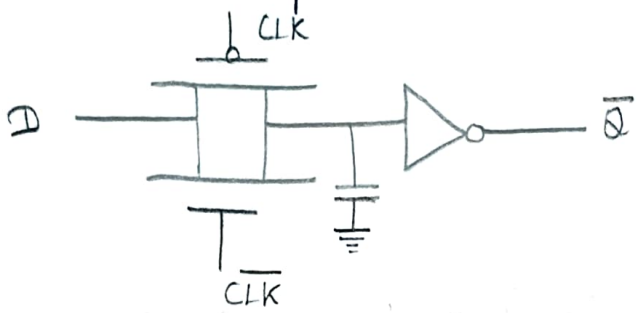
i) Dynamic latches

=> when CLK is 0, the latch is transparent.

data D is stored on the capacitance C_1. If the input D is 1, charge is present on the capacitance and absence of charge denotes a 0 input.

=> When CLK is 1, the latch is in opaque mode and the output Q is same as the previous value.

=> This latch produces an inverted output



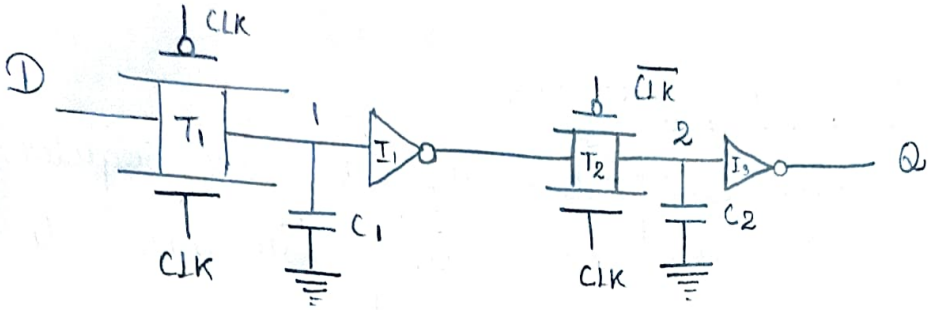
Dynamic Transmission - Gate Edge - triggered Registers

* It is a fully dynamic positive edge - triggered register based register master slave concept.

* This implementation of an edge - triggered register is very efficient as it requires only 8 transistors.

* The sampling switches can be implemented using NMOS - only pass transistors resulting in an even simpler 6 transistor implementation.

* The reduced transister count is attractive for high performance and low power systems.



* The setup time of this circuit is simply the delay of the transmission Gate and corresponds to the time it takes node 1 to sample the D input.

* The hold time is approximately Zero, since the transmission Gate is turned off on the clock edge and further inputs changes are ignored.

* The propagation delay is equal to two inverter delays plus the delay of the transmission Gate T_2.

Disadvantages of Dynamic Registers:

i) Storage nodes has to be refreshed at periodic intervals to prevent loss due to charge leakage, due to diode leakage as well as subthreshold currents.

ii) Clock overlap - It is an obviously an undesirable effect.

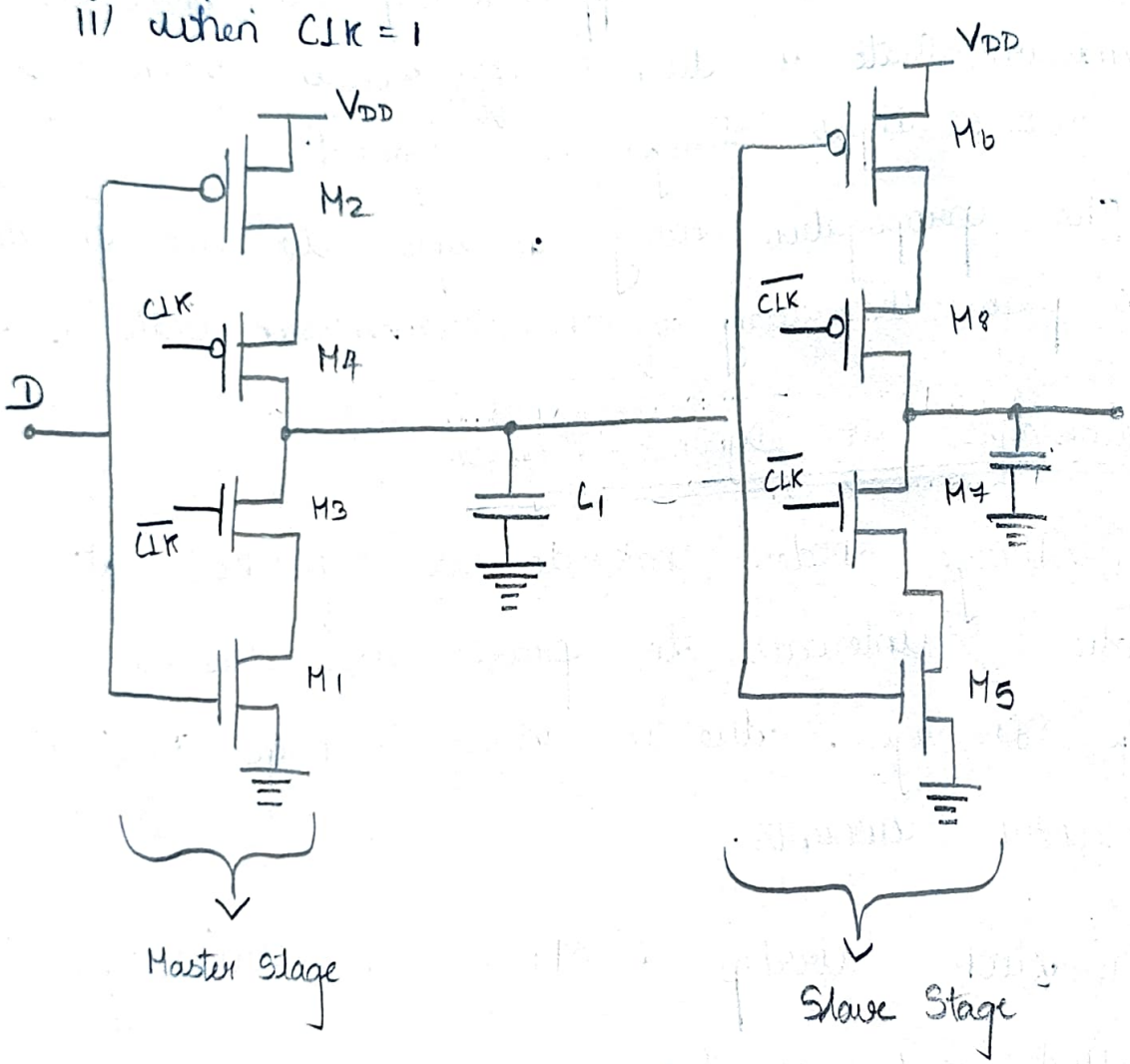
C^2MOS (Clocked CMOS) Register :

★ An ingenious positive edge - triggered register, based on a master slave concept insensitive to clock overlap.

★ This circuit is called the C^2MOS (Clocked CMOS) register and operates in two Phase.

i) $CLK = 0$ $(\overline{CLK} = 1)$

ii) when $CLK = 1$



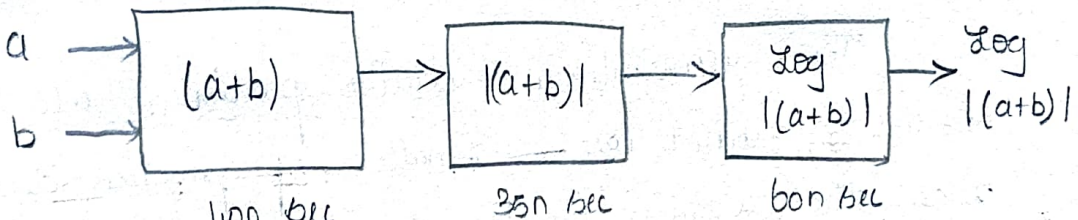
Pipelining :

* Pipelining is a popular design technique often used to accelerate the operation of the data paths in digital process.

* The major advantage of pipelining are to reduce glitching in complex logic networks and getting lower-energy due to operand isolation.

* The application are pipelining combinational/ Algebraic operations.

* The process can be represented pictorially.



Out = log |(a+b)|.

Computation of out :

clock Period	Adder	Absolute value	Log
1	a_1+b_1		
2	a_2+b_2	$\|a_1+b_1\|$	
3	a_3+b_3	$\|a_2+b_2\|$	$\log\|a_1+b_1\|$
4	a_4+b_4	$\|a_3+b_3\|$	$\log(\|a_2+b_2\|)$
5	a_5+b_5	$\|a_4+b_4\|$	$\log(\|a_3+b_3\|)$

The minimal clock period Tmin,

$$T_{min} = t_{pcq} + t_{pd} + t_{setup}$$

where t_{pcq} } --> Propagation delay.
t_{setup}] --> setup time

Pipelining is a technique to improve the resource utilization, and increase the functional throughput.

The advantage of pipelined operation becomes apparent when examining the minimum clock period of the modified circuit.

The combinational circuits partioned into three sectors, which has a smaller propagation delay than the original function.

$$T_{min,pipe} = t_{pcq} + \max(t_{pd,add}\ t_{pd,ads}\ t_{pd,}$$

Timing classification of Digital systems:

Timing Parameters for combinational Logic:

Propagational Delay (t_{pd}):

The amount of time needed for a change in a logic circuit result in a permanent change at an output, that is the combinational logic will

show any further output changes in response to an input change after time t_{pd} units.

Contamination Delay (t_{cd}):

The amount of time needed for a change in a logic input to result in an initial change at an output. that is the combinational logic guaranteed not to show any output change in response to an input change.

Timing Parameters for Sequential logic:

Setup time (t_{setup}):

The amount of time before the clock edge that data input D must be stable the rising clock edge arrives.

Clock Skew and Jitter:

clock Skew t_{SK}:

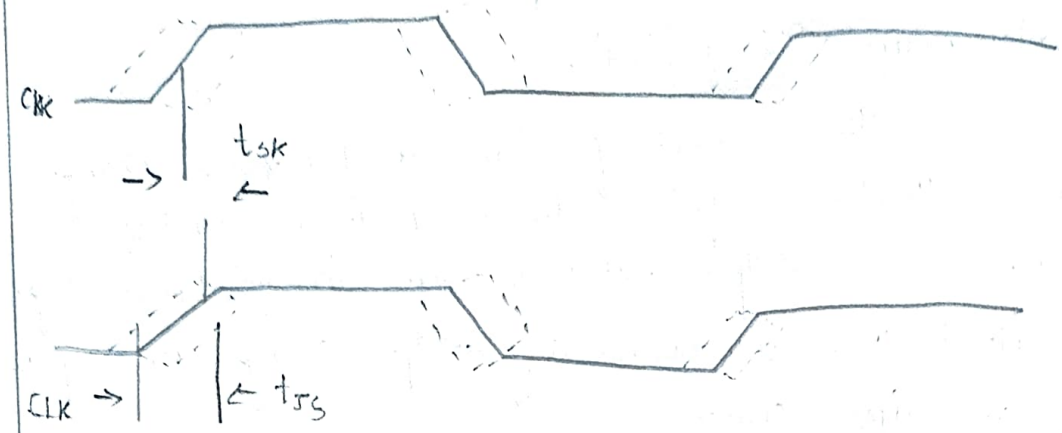
Spatial Variation in temporally equivalent clock edges; deterministic + random

Clock Jitter:

Temporal Variation in consecutive edges of the clock signal modulation + random noise cycle to cycle (short term) t_{JS} long term t_{JL}.

⇒ Both Skew and Jitter affect the effective cycle time, but only Skew affects the race Margin.

Synchronous Interconnect : Clock Skew and Jitter

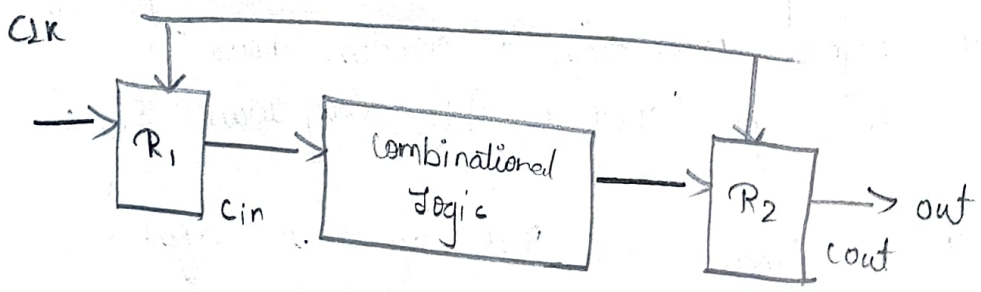


Synchronous Interconnect :

A synchronous signal is with the exact same frequency and a known fixed phase offset with respect to the local clock.

This signal is "synchronised" with the clock and the data can be sampled directly without any uncertainity.

In digital logic design, synchronous systems are the most straightforward type of interconnect, where the flow of data in a circuit.



Synchronous Timing Basics:

* The contamination (minimum) delay t_{ccq}, and maximum propagation delay of the register t_{pcq}.

* The set up (t_{setup}) and hold time (t_{hold}) for the registers.

* The contamination delay t_{cd} and maximum propagation delay t_{pd} of the combinational logic.

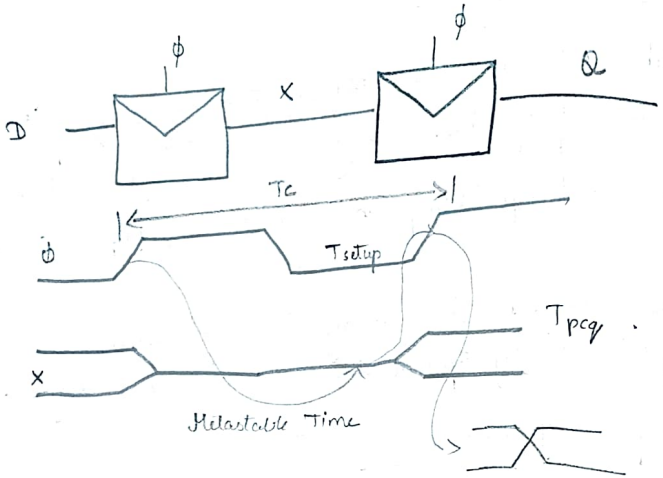
A Simple Synchronizer:

* A synchronizer accepts an input D and a clock ϕ.

* It produces an output Q that should to be valid some bounded delay after the clock.

* The synchronizer has an aperture defined by a setup and hold time around the rising edge of the clock.

* If the data is stable during the aperture Q should be equal D. If the data changes during the aperture, Q can be choosen arbitarily.



If the synchronizer receives an average of N asynchronous input changes at D each second, the probability of synchronizer failure in any given second is,

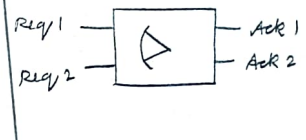
$$P(\text{failure}) = N T_0 e^{-\frac{(T_c - t_{setup})}{\tau_s}}$$

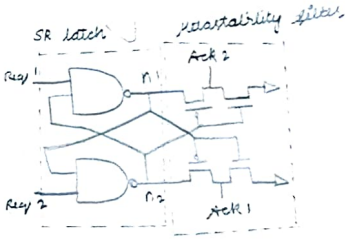
and the mean time between failures increases exponentially with cycle time.

$$MTBF = \frac{1}{P(\text{failure})} = \frac{T_c e^{\frac{T_c - t_{setup}}{\tau_s}}}{N T_0}$$

Arbiters :

An arbiter is an element that decides which of two events has occured first. If the spacing between the input exceeds some aperture time, the first input should be acknowledged. If the spacing is smaller, exactly one of the two inputs should be acknowledged, but the choice is arbitrary.





Unit - IV

Interconnect, Memory Architecture and Arithmetic circuits.

Interconnect Parameters - Capacitance, Resistance and Inductance, Electrical Wiremodels, Sequential digital circuits: adders, multipliers, comparators, shift registers. Logic implementation using Programmable devices (ROM, PLA, FPGA), Memory Architecture and Building Blocks, Memory core and Memory Phreripherals circuitry

Introduction:

Data path is the place where the microprocessor executes operation such as Addition, Subtraction shifting, Rotating and Boolean logical function on data.

Execution of an operation on the two selected operands and placement of the result in a register The elements of the datapath must be designed to facilitate such operations.

Interconnect Parameters:

chips are mostly made of wires

Wires are as important as transistors

- Speed
- noise
- power

Alternating layers run orthogonally.

Pitch = W+S.

Aspect ratio: AR = t/W

- old process had AR << 1
- Modern process have AR = 2.

Sequential digital circuits:

Addition is a fundamental operation of any digital system, digital signal processing of control system.

A fast and accurate operations of a digital system is generally influenced by the performance of the resident adders.

Also adders are very important component in digital systems because of their extensive use in implementing other basic digital systems because of their extensive implementation.

Classification of Adders:

The adders are classified as,

* Ripple carry adder
* Carry look ahead adder
* Carry skip adder
* Manifest chain adder
* Carry select adder
* Pre-fix Adders
* Multi operand Adder
* Carry save Adder
* Pipelined parallel Adder.

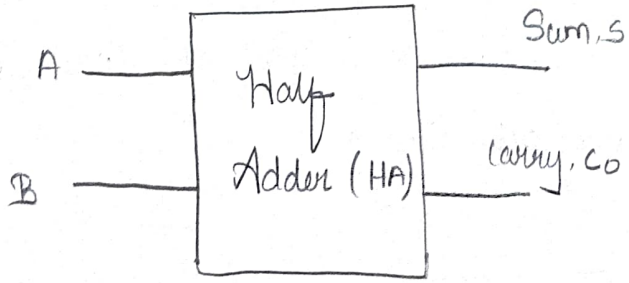
Basic Adder:

Half Adder:

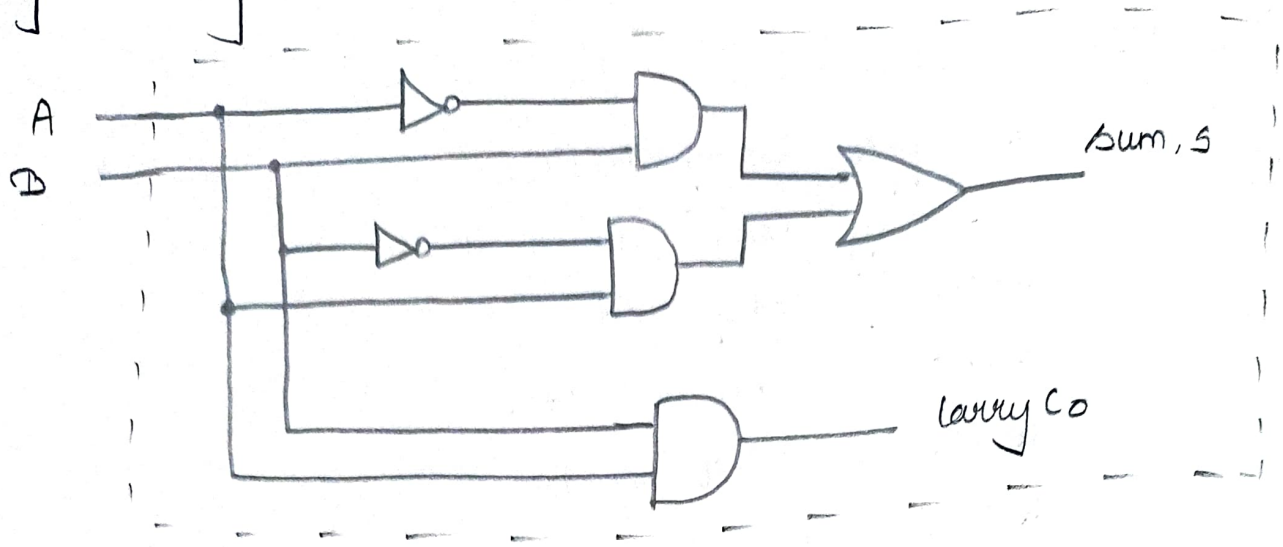
A half Adder is used to add two binary digits, A and B.

It produces S - the sum of A and B, and the corresponding carry out C_o.

Block Diagram:



Logic Diagram:



Truth Table

A	B	S	C_o
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Boolean Equation:

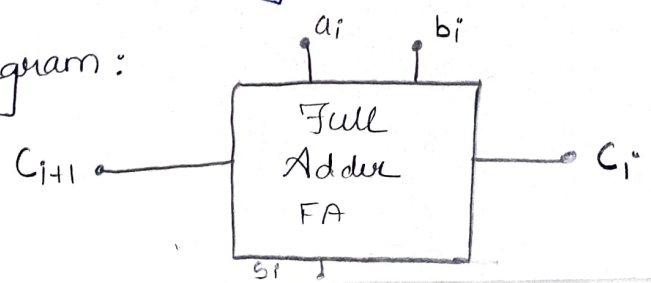
$$S = A \oplus B$$

$$C_o = AB$$

Full Adder:

A full adder is a combinational circuit that performs the arithmetic sum of three bits: a_i, b_i and a carry out C_{i+1}.

Block Diagram:



Boolean Equation :

$$S_i = a_i \oplus b_i \oplus c_i$$

$$C_{i+1} = a_i b_i + c_i (a_i \oplus b_i)$$

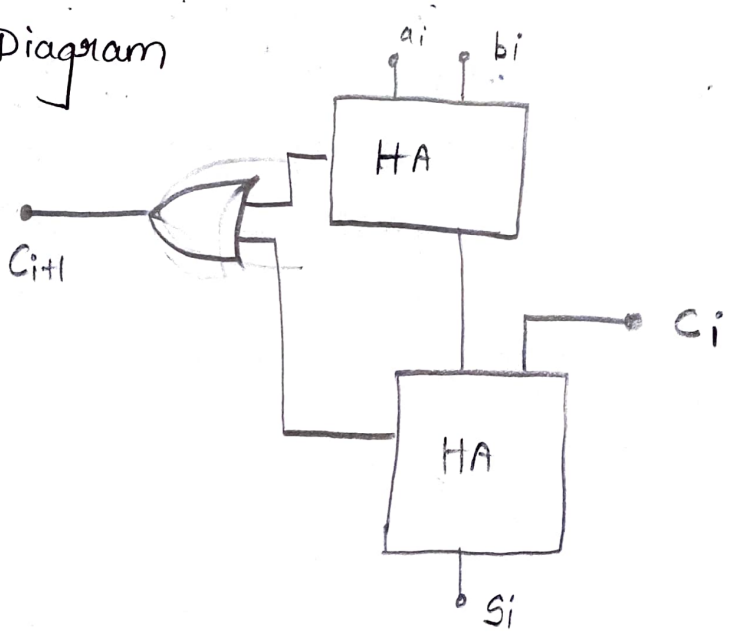
(or)

$$C_{i+1} = a_i b_i + c_i (a_i + b_i)$$

Truth Table :

a_i	b_i	c_i	S_i	C_{i+1}
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	0	1

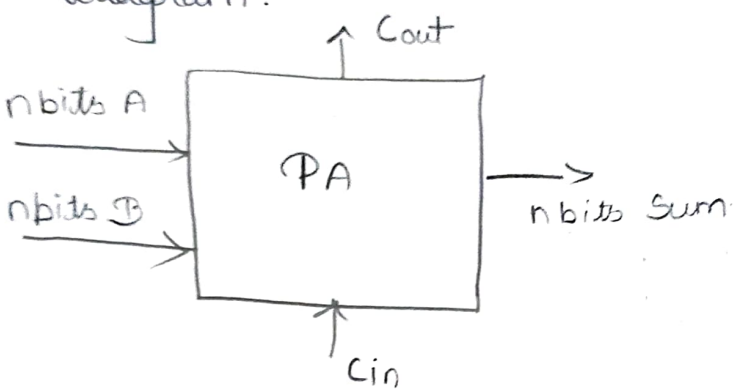
Logic Diagram



Parallel Adders:

Parallel Adders are digital circuits that compute the addition of variable binary strings of equivalent or different size in parallel.

Block diagram:

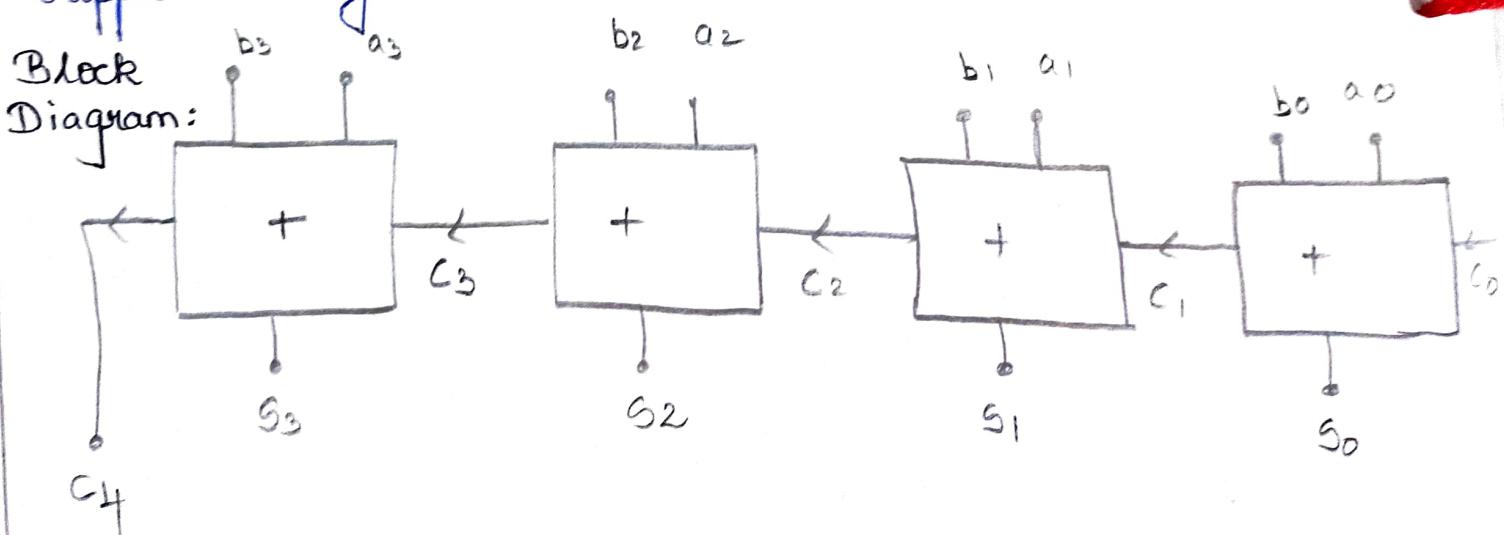


i) Ripple carry adder:

The ripple carry adder is constructed by cascading full adder (FA) blocks in series.

One full adder is responsible for the addition of two binary digits at any stage of the ripple carry.

Block Diagram:



Carry look ahead Adder:

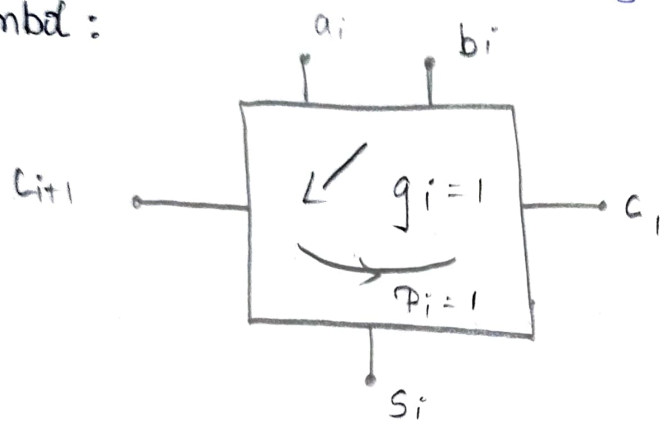
Carry look ahead Adder solves the limiting factor problem by calculating the carry signals in advance, based on the input signals.

The Propagate P_i and Generate g_i signals, are

$P_i = a_i \oplus b_i$, carry propagate

$g_i = a_i b_i$, carry generate.

Symbol:



Manchester Adder:

The propagation time, when calculating the sum of two binary strings A and B using any generic parallel adders, can be sped up significantly if we utilize a Manchester cell in a design of that particular adder.

The carry propagation circuitary can be simplified by adding delete and generate signals

The condition for a carry generate (generation of a new carry) to occur at any stage of the condition of the addition is $A_i = B$ making the carry out C_{i+1}, depends solely on G_{ii}, A carry propagate, $A_i \oplus B_i$ hence producing $C_{i+1} = C_i$.

Boolean Equation :

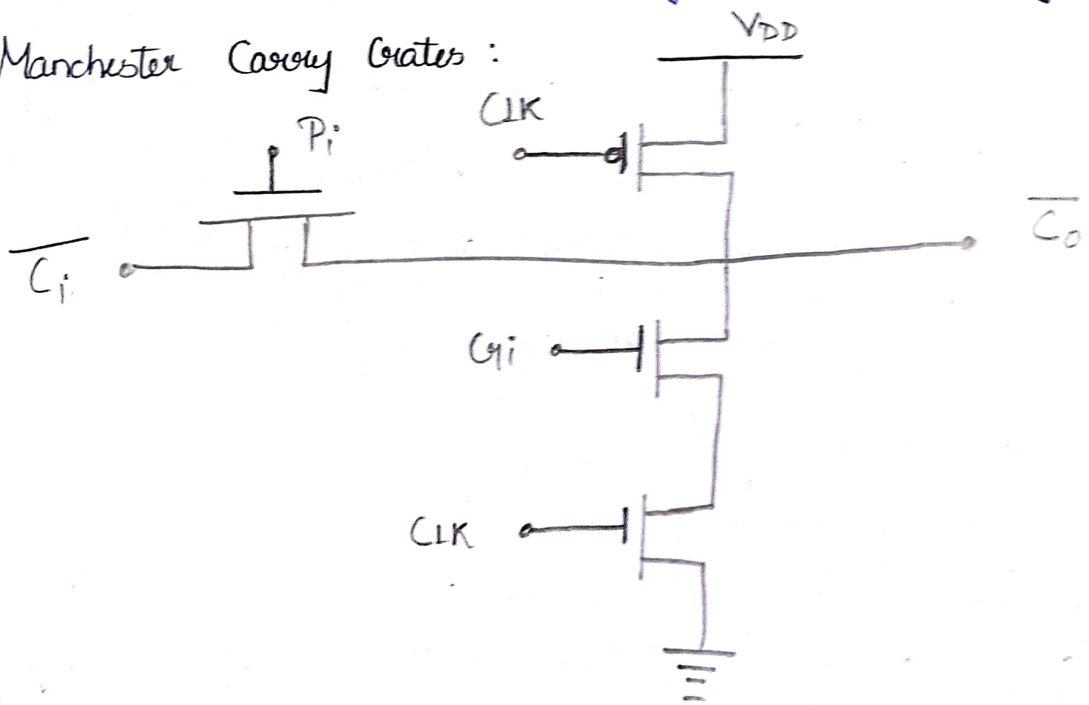
$G_{ii} = A_i B_i$ – carry generate of ith stage

$P_i = A_i \oplus B_i$ – carry propagate of ith stage

$S_i = P_i \oplus C_i$ – Sum of ith stage

$C_{i+1} = G_{ii} + P_i C_i$ – carry out ith stage

Manchester Carry Crates :



Aj	Bi	Pi	Gi	ki
0	0	0	0	1
0	1	1	0	0
1	0	1	0	0
1	1	0	1	0

Multiplier :

Multiplication is a heavily used arithmetic operation that figures prominently in signal processing and scientific applications.

Multiplication is hardware intensive.

Main criteria are,

-> higher speed

-> Lower cost

-> Less VLSI area.

a_1 b_1 ——> Multiplicand

a_0 b_0 ——> Multiplier

---

a_1b_0 b_0b_1 ——> Partial products

a_0a_1 a_0b_1

---

d c b b_0b_1 ——> output.

Types of Multiplier:

i) Array Multiplier:

* Used in unsigned numbers using an array of CSA's.

* The generation of a partial products requires N * M two bit AND gates.

* Most of the area of the Multiplier is devoted to the adding of partial products.

* The shifting of the partial products for their proper alignment's performed by simple routing.

* The adder can easily be pipelined with the placement of registers between rows.

Carry look-ahead adder

* In ripple carry adder, its limiting factor is the time it takes to propagate the carry.

* The carry look-ahead adder solves this problem by calculating the carry signals in advance based on i/p signals

* As a result reduced carry propagation time can be achieved.

* Here we have to manipulate the sum S_i, and carry C_{i+1} expression in terms of propagate P_i and generate g_i signals

Propagate P_i and generate g_i signals is given as:

$P_i = a_i \oplus b_i$, P_i => Carry propagate

$g_i = a_i b_i$, g_i => Carry generate

	g_i	P_i
	$a_i b_i$	$a_i \oplus b_i$
$a_i = b_i = 0$	0	0
$a_i = b_i \neq 1$	1	0
$a_i \neq b_i$	0	1

$$C_{i+1} = a_i \cdot b_i + C_i \cdot (a_i \oplus b_i)$$

i)

* Both propagate and generate signals depend only on the input bits & thus will be valid after one gate delay

output Sum and carry-out is given by

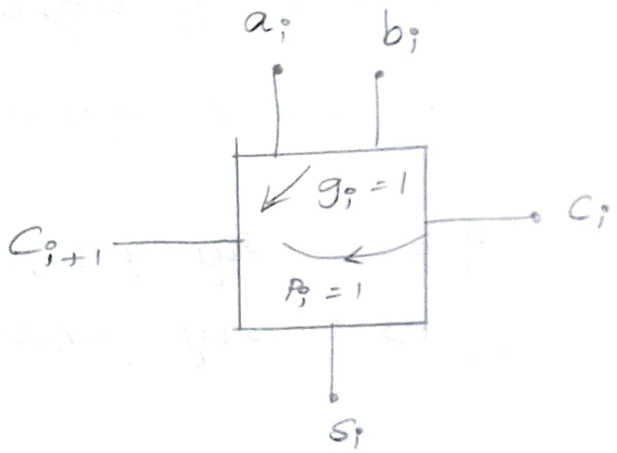
$$S_i = P_i \oplus C_i$$

$$C_{i+1} = g_i + P_i C_i$$

carry signal generated in 2 cases

① If both bits a_i and b_i are 1

② If either a_i or b_i is 1 and the carry-in C_i is 1



where $i = 0, 1, 2, 3$

For 4-bit adder, the carry equations are

$$C_1 = g_0 + P_0 C_0$$

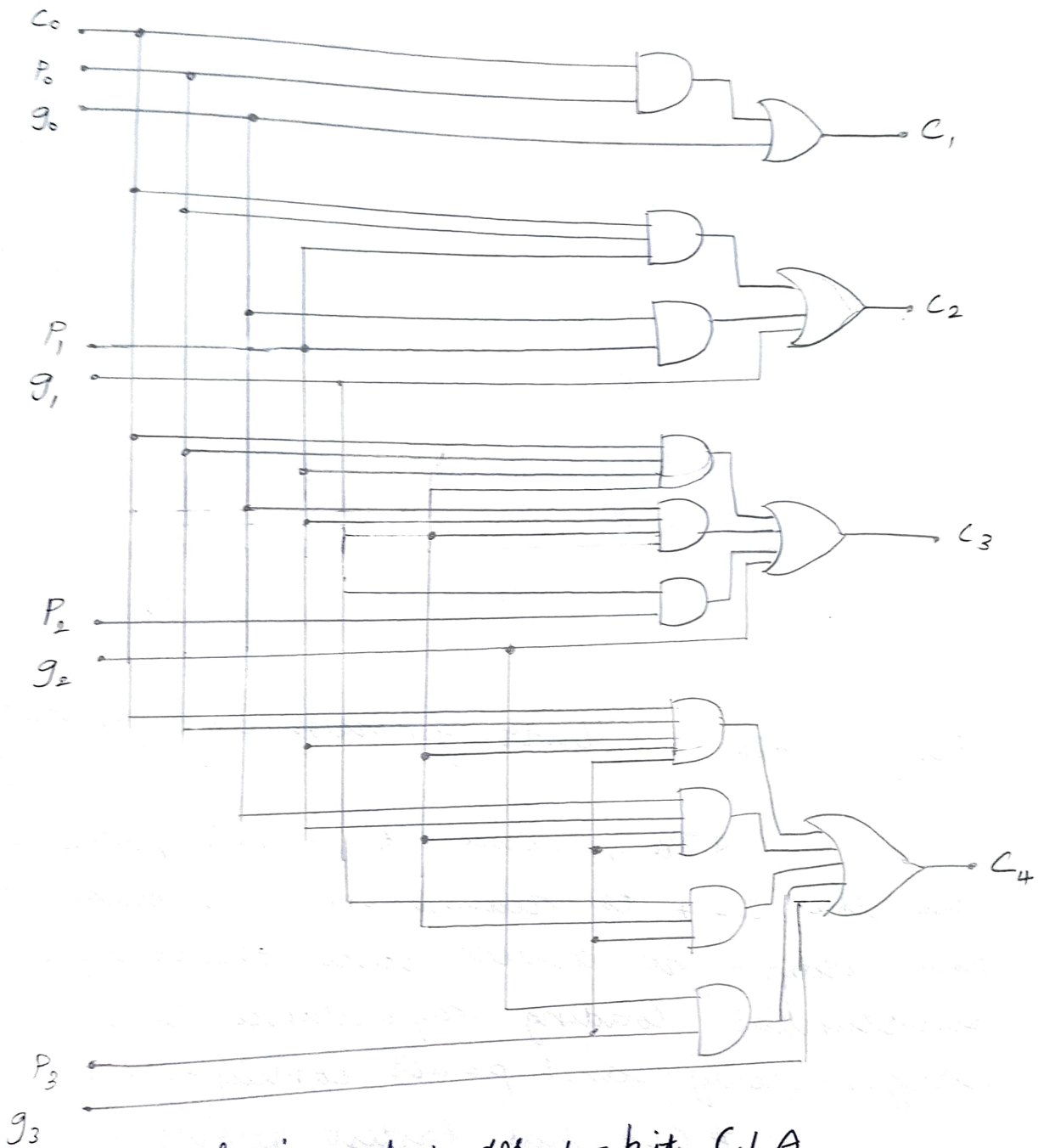
$$C_2 = g_1 + P_1 C_1 = g_1 + P_1(g_0 + P_0 C_0) = g_1 + P_1 g_0 + P_1 P_0 C_0$$

$$C_3 = g_2 + P_2 C_2 = g_2 + P_2(g_1 + P_1 C_1) = g_2 + P_2 g_1 + P_2 P_1 g_0 + P_2 P_1 P_0 C_0$$

$$C_4 = g_3 + P_3 C_3 = g_3 + P_3(g_2 + P_2 C_2) = g_3 + P_3 g_2 + P_3 P_2 g_1 + P_3 P_2 P_1 g_0 + P_3 P_2 P_1 P_0 C_0$$

general expression for N-bit adder is

$$C_{i+1} = G_i + P_i G_{i-1} + P_i P_{i-1} G_{i-2} + \dots P_i P_{i-1} \dots P_2 P_1 G_0 + P_i P_{i-1} \dots P_1 P_0 C_0$$



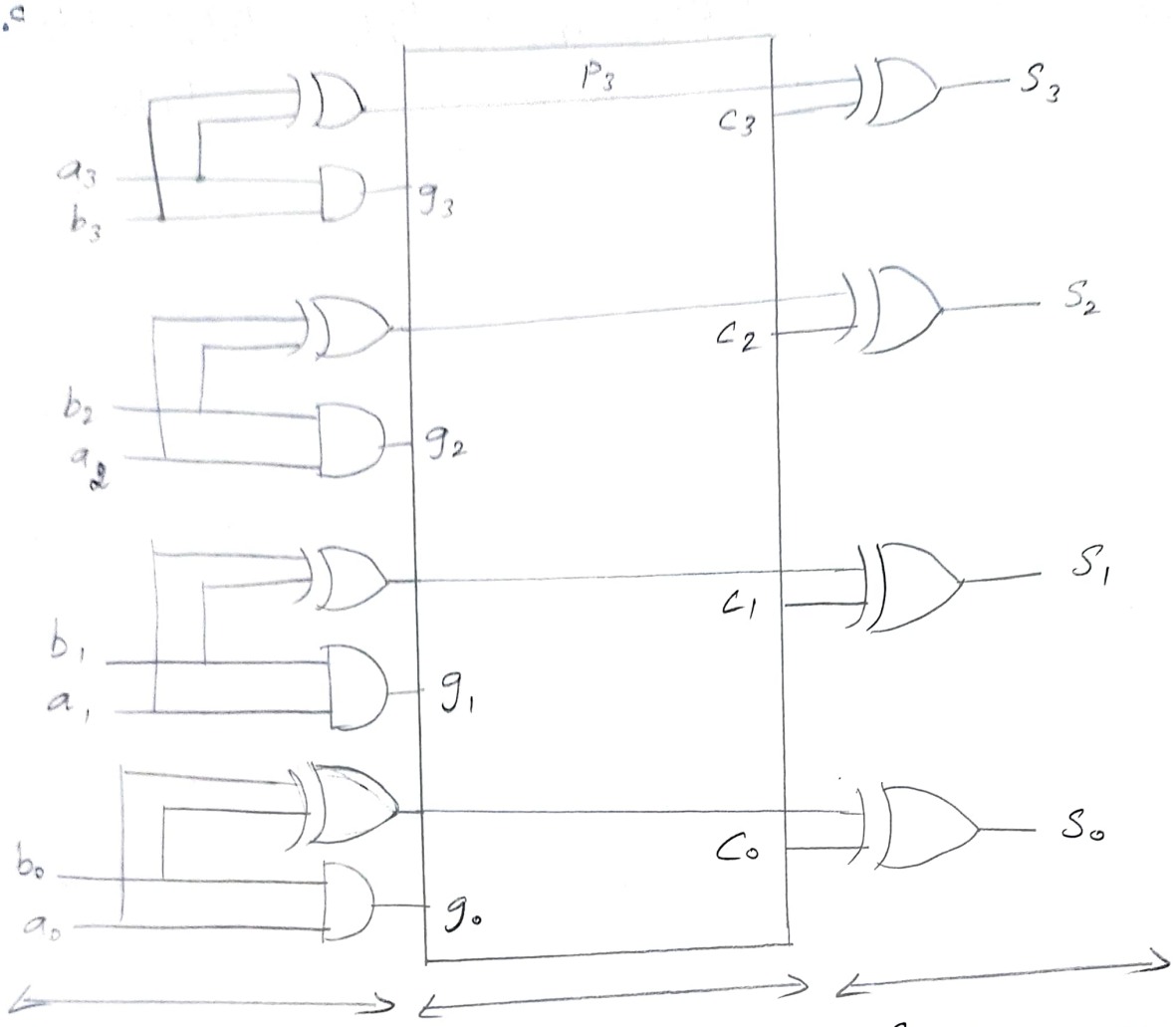
Logic N/W for 4-bit CLA

A Carry look ahead adder's structure can be divided into three parts.

(i) The propagate / generate generator

(ii) The sum generator

(iii) The Carry generator.



* In practice, it is not possible to use the CLA to realize constant delay for the wider-bit adders since there will be substantial loading capacitance, and hence larger delay and power consumption

* CLA has fastest growing area and Power requirements with respect to bit size

* Speed will drop with increase in bit size.

Braun Multiplier :

* The simplest parallel Multiplier is the Braun Array.
* All the partial products are computed in parallel.
* Then collected through a cascade of carry save adders.
* The completion time is limited by the depth of the carry save adder and by the propagation of the adder.
* This Multiplier is suited for positive operands.
* It constructs only by the half adders and full adders.
* Output is taken from the previous Multiplier bit.
* So it is named as simplest parallel adder.

i)

Logic implementation using programmable devices:

Programmable devices are the standard IC's which can be programmed to implement the desired functions.

The important features of the PLD's are,

→ No customized mask layer or logic cells.

→ Fast design turnaround.

→ A single large block.

→ A Matric of logic macro cells.

Types of PLD's,

* Read only Memory (ROM)
* Programmable array logic (PAL)
* Programmable Logic Array (PLA)

ROM:

The simplest type of programmable IC's is a read only Memory.

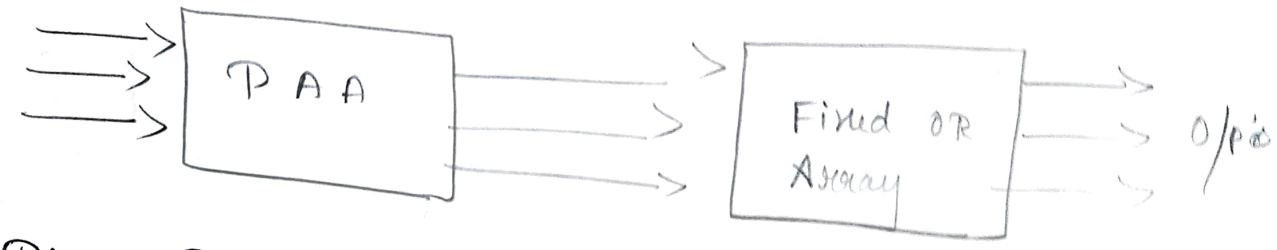
→ Metal fuse that can be blown permanently.

Programmable ROM or Prom

PAL: Programmable Array logic

→ Programmable AND Array

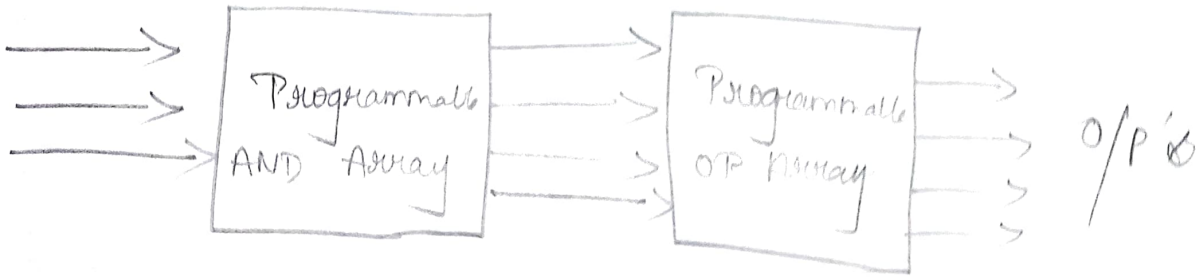
→ Fixed OR Array



PLA: Programmable logic Array

→ Programmable AND Array

→ " OR Array.



FPGA: Field Programmable Gate Array:

It is the newest member of ASIC family and are rapidly going in and replacing TTL in a microelectronic system.

FPGA is a gate array, contains a regular system of programmable basic logic cells.

The important characteristics of FPGA are,

-> None of the masks layers are customized.

-> A Method for programming the logic cells and the interconnect.

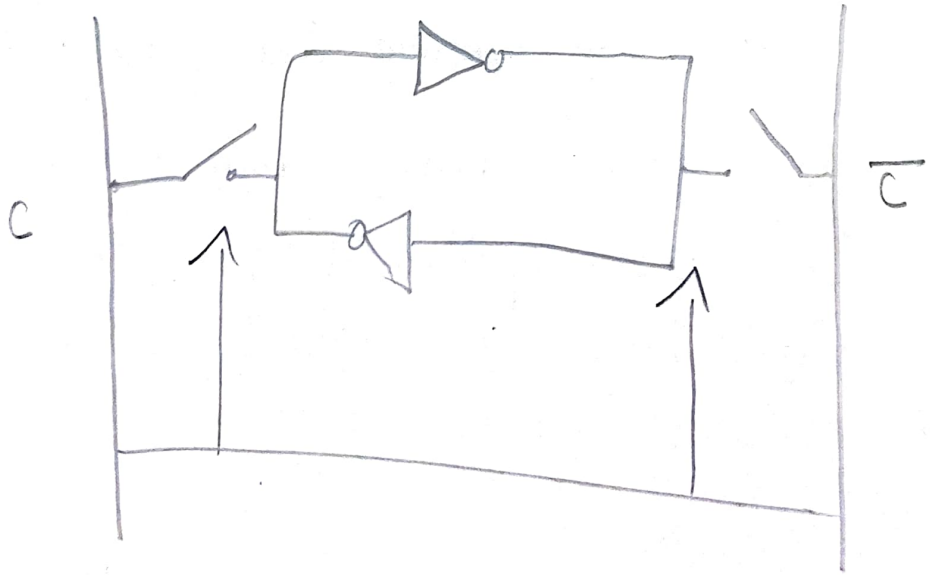
->The core is a regular array of programmable logic cells that can implement combinational as well as sequential logic.

->A Matrix of programmable interconnect

->Programmable I/O cells surround the core.

->Design turnaround is a few hours.

Static RAM:



READ operation:

* Consider a read operation, assuming that logic '0' is stored in the cell.
* The transistors M_2 and M_5 are turned off.
* while the transistors M_1 and M_6 operate in linear mode.
* Thus internal Voltage are $V_1 = 0$, $V_2 = V_{DD}$ before the cell access transistors are turned on.
* After the pass transistors M_3 and M_4 are turned on by the row selection circuitary, the Voltage CBb of will not change any significant Variation.
* Therefore the Voltage must be not exceed the threshold Voltage of M_2.
* The transistors M_2 remained turn off during the read phase.
* It is the read operation.

SRAM write circuitary :

$\overline{W}$	Data	WB	$\overline{WB}$
0	1	1	0
0	0	0	1
1	X	0	0

→ M_1 - off . M_2 - on V_c high $V_{\bar{c}}$ - low

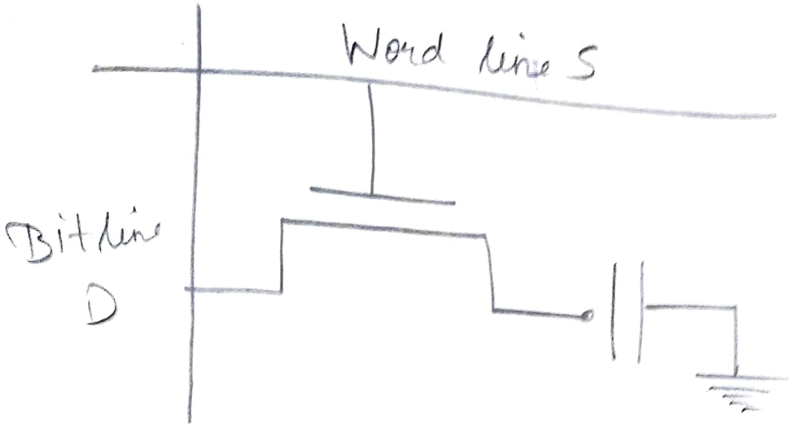
→ M_1 - on . M_2 off , V_c low , $V_{\bar{c}}$ high

→ M_1 . M_2 off . V_c , $V_{\bar{c}}$ high

M_1 → is the only in the presence of the write enable signal ($\overline{W} = 0$) when the data is written to be 0

M_2 transistors → is the only in the presence of the write signal ($\overline{W} = 0$) when the data bit to be written as '1'.

Dynamic Read Write Memory (DRAM)



In dynamic RAM binary data is stored as charge in a capacitor.

It is retained for the limited time due to the leakage current.

Therefore call the periodic refreshing of the stored data before unwanted stored charge modification occurs.

Unit-5

ASIC design and Testing

Introduction to wafer to chip Fabrication process flow Microchip design process & issues in test and verification of complex chips, embedded cores and SOC's Fault models. Test coding. ASIC design Flow, Introduction to ASIC's. Introduction to test benches Writing test benches in Verilog HDL, Automatic test pattern generation. Design for testability. Scan design: Test interference and boundary Scan.

Introduction to wafer to chip Fabrication process:

Introduction:

Metal - oxide - Semiconductor (MOS) fabrication is the process used to create the Integrated circuits (ICs) that are presently used to realize electronic circuits. It involves multiple steps of photolithographic and chemical processing steps during which electronic circuits are gradually created on a wafer made of pure semi conducting material.

Silicon is always used, but various compound Semiconductors such as gallium - arsenide.

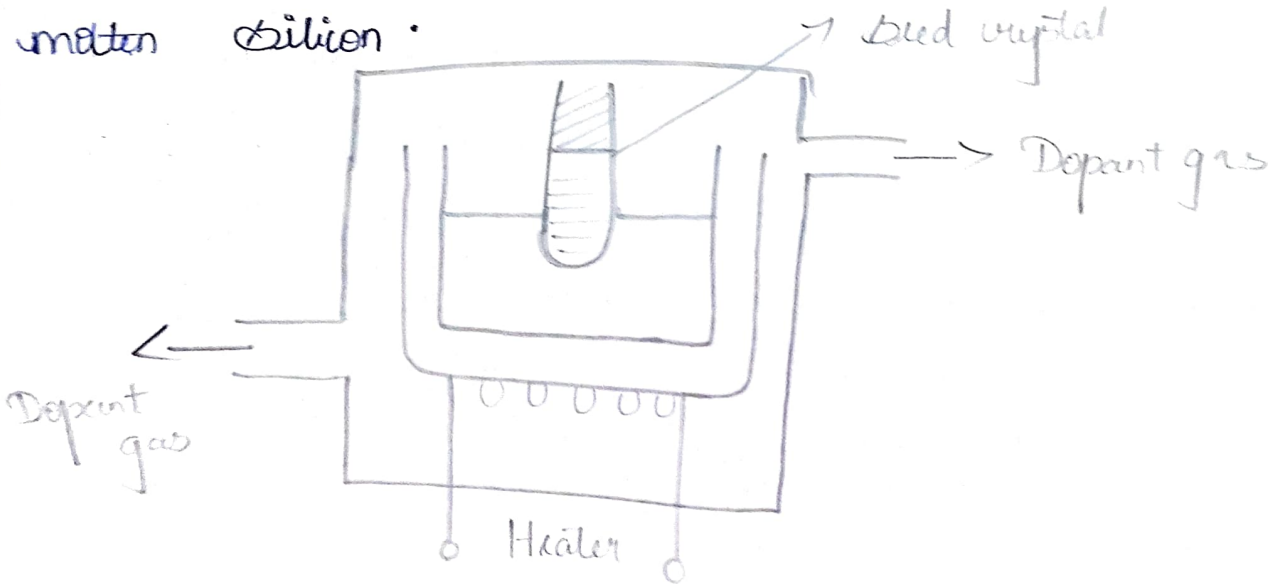
Wafer Fabrication:

The MOS fabrication process starts with a thin wafer of silicon. The raw material used for obtaining silicon wafer is sand or silicon dioxide.

Sand is a cheap material and it is available in abundance on earth.

It has to purified to a high level by reacting with carbon and then crystallized by an epitaxial growth process.

The purified silicon is held in molten state at 1500°C and seed crystal is slowly with drawn after dipping in contact with the molten silicon.



Isolation :

* Individual devices in a CMOS process need to be isolated from one another so that they do not have unexpected interactions.

* The source and drain of transistors form reverse biased p-n junctions with the substrate or well, isolating them from their neighbours.

* The formation of any parasitic MOS channels must be prevented.

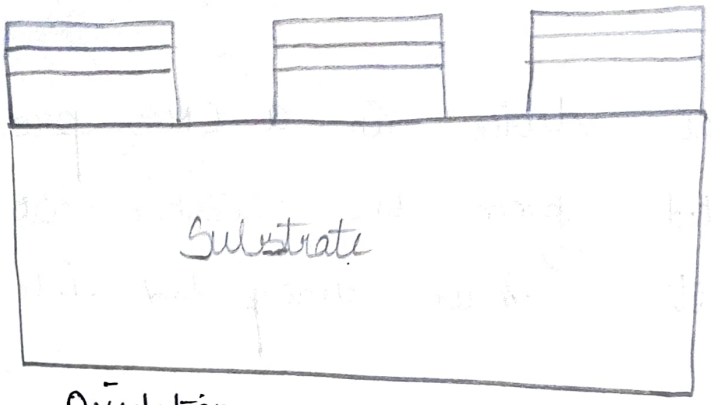
* This is commonly achieved using a thin gate oxide for the transistors and much thicker field oxide elsewhere.

* The thicker oxide increases the threshold voltage to the value above the supply voltage.

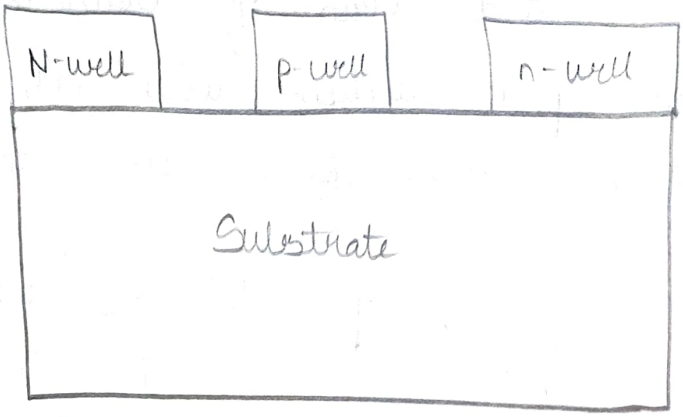
* It prevents the channel from forming in the substrate unless there is an over voltage condition.

* In early metal gate process that had a uniform oxide layer, the channel stop diffusion surrounded each transistor.

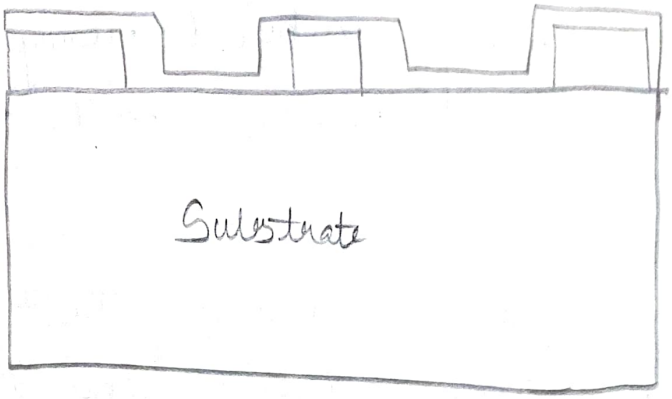
i) Trench Oxide :



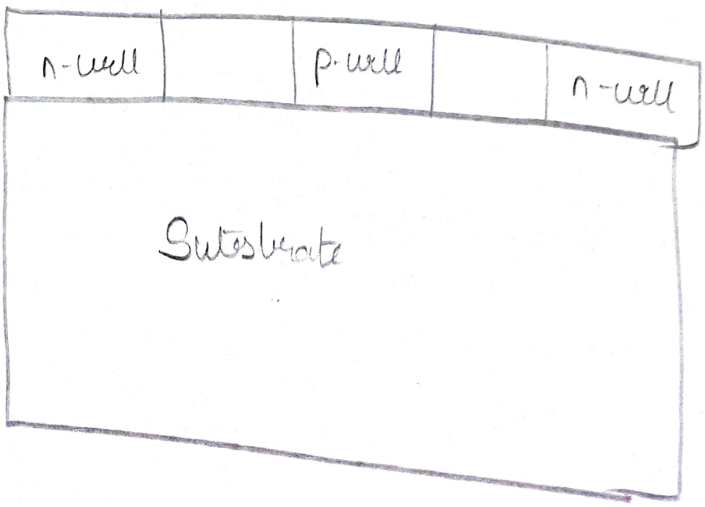
ii) Linear Oxidation



iii) Fill trench :



iv) CMP



Gate and Source / Drain Formation:

★ While silicon is deposited on SiO_2 or other surfaces without crystal orientation, it forms polycrystalline silicon commonly or simple poly.

★ An annealing process is used to control the size of the single crystal domains to improve the quality of the polysilicon.

★ Undoped polysilicon has high resistivity.

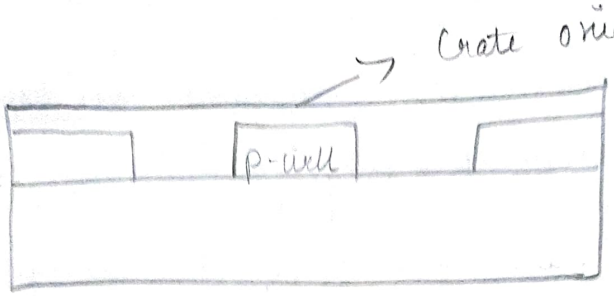
★ The resistance can be reduced by implanting it with dopants and / or combining it with a refractory metal.

★ The polysilicon gate with a serves as a mask to allow precise alignment to the source and drain with the gate.

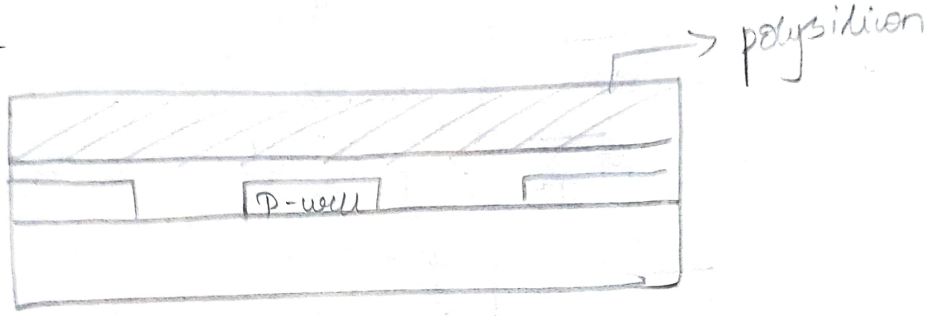
★ This process is called a self aligned polysilicon gate process.

★ Aluminium would not be used because it would melt during formation of the source and drain.

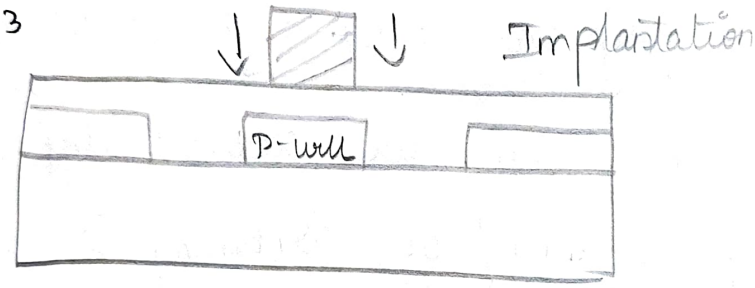
Step: 1



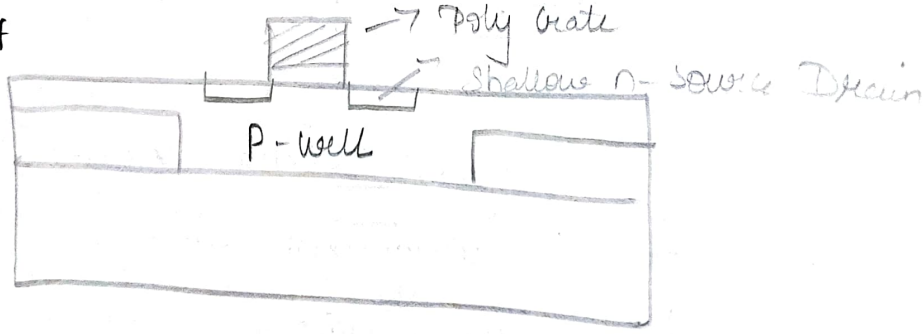
Step: 2



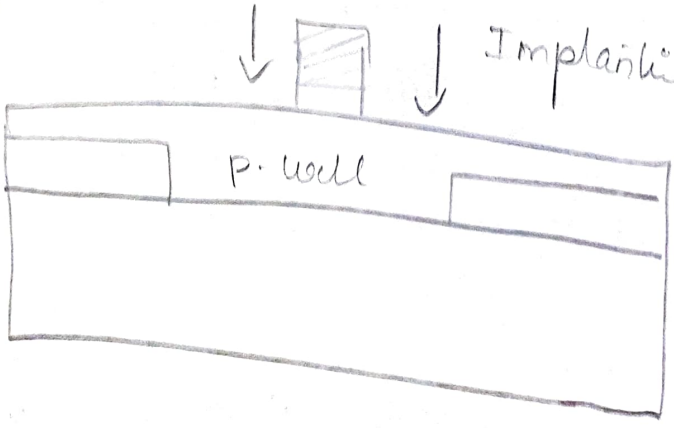
Step: 3



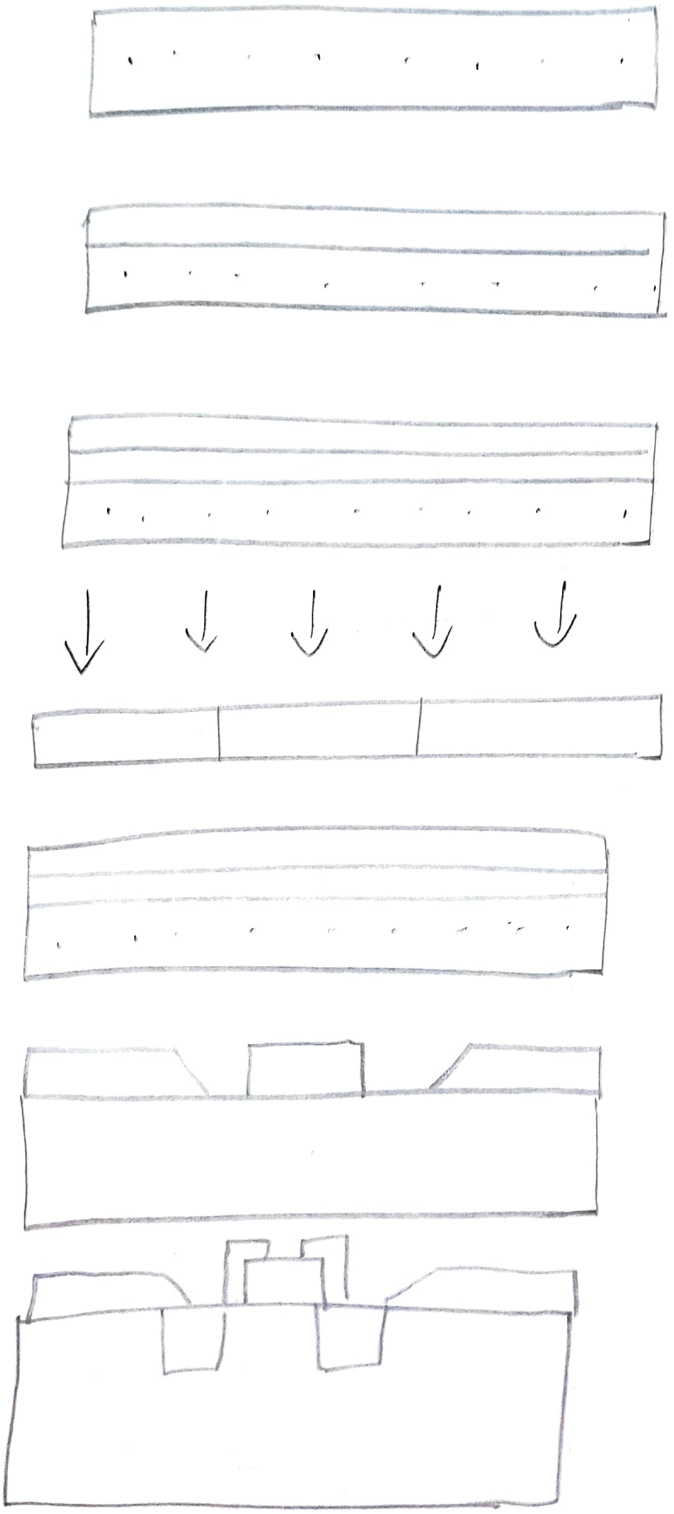
Step: 4



Step: 5



N- Mos fabrication steps :



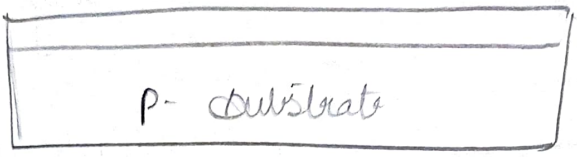
Thick oxide layer

Photoresist

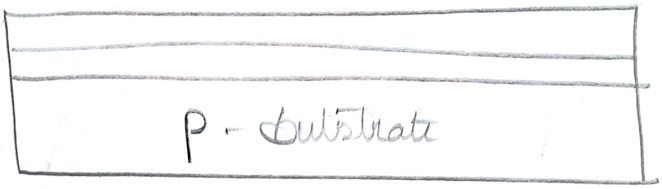
CMOS fabrication steps:

The N- well process:

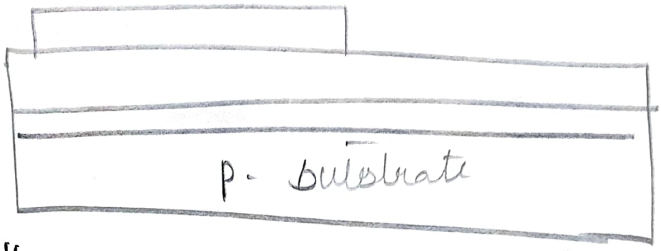
Step: 1



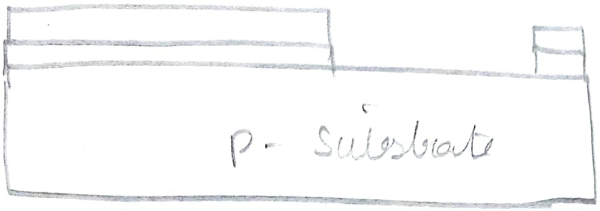
Step: 2



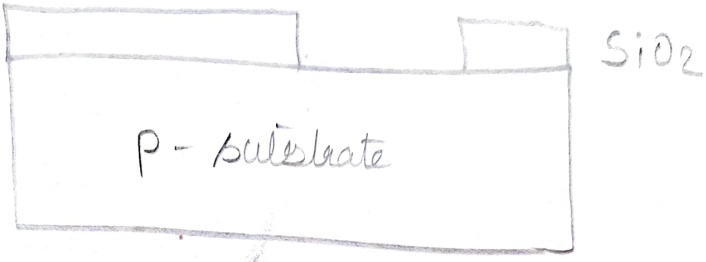
Step: 3



Step: 4



Step: 5



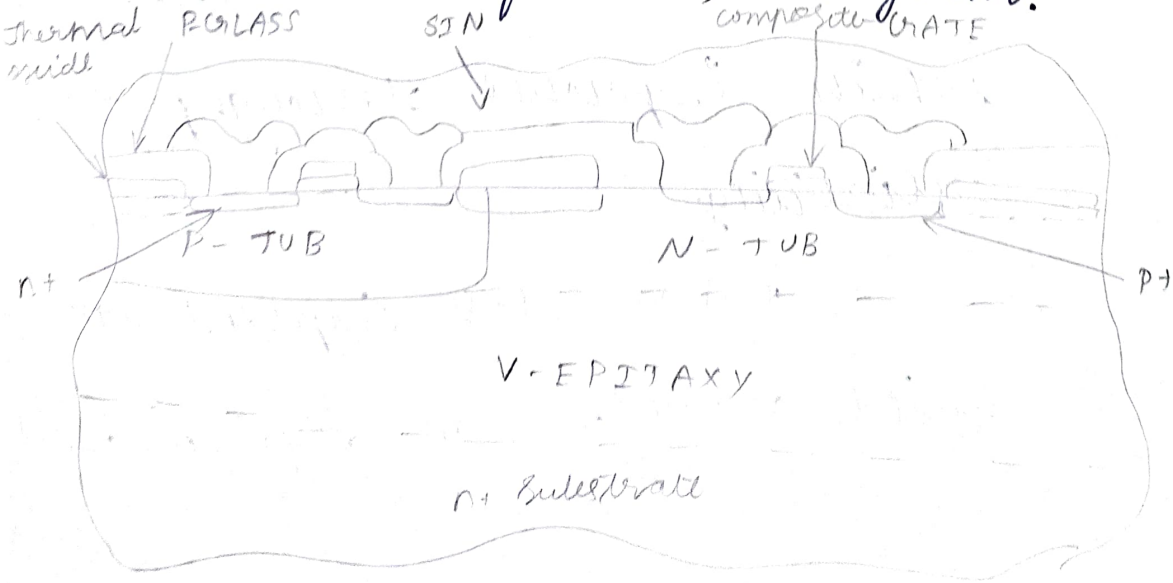
Twin-tub process

* Twin tub CMOS technology provide the basis for seperate optimization of the p-type and n-type transistors, thus making it possible for threshold voltage, body effect and the gain associated with n- and p- devices to be independently optimized.

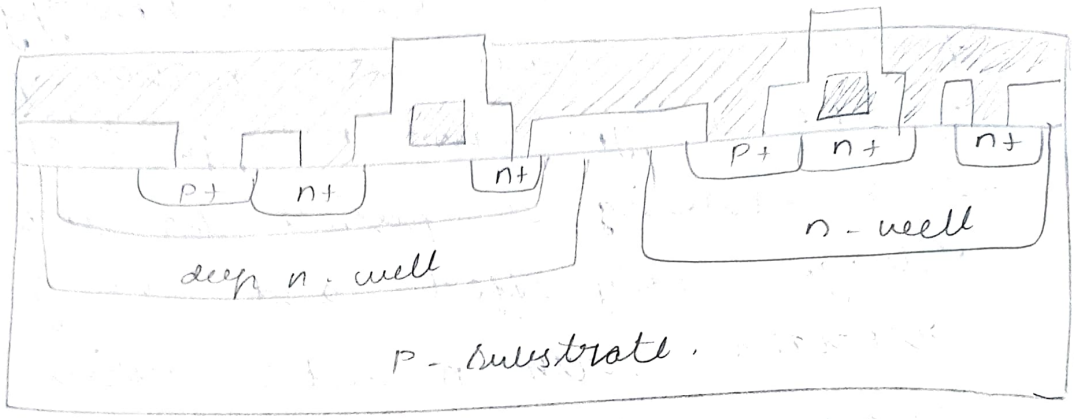
* The electrical properties for this layer are determined by the dopant and its concentration in the silicon.

* This is similar to p-well process apart from the tub formation where both p-well and n-well are utilized. entails the following steps:

i) Tub formation ii) Thin oxide etching iii) Source and drain implantations iv) Contact cut definition v) Metallization.



Triple Well Process.



* The first step in most CMOS processes is to define the well regions.

* In a triple well process, a deep n-well is first driven into the P-type substrate, usually using high energy ion implantation as opposed to a thermally diffused operation.

* This avoids thermal cycling, which improves throughput and reliability.

* A 2-3 MeV implantation can yield a 2.5-3.5 μm deep n-well.

ASIC design Flow:

Design entry: Enter the design into an ASIC design system, either using a hardware description language

-> Logic synthesis
-> System partitioning
-> Prelayout simulation
-> Floorplanning
-> Placement.
-> Routing
-> Extraction
-> Postlayout simulation

Design Entry:

★ It describes the RTL (Register transfer level) logics in HDL's.

★ For this, we use many of the hardware description languages.

Logic synthesis:

★ The RTL logic written is synthesized to get the gate level netlist.

★ This process can be done with help of EDA tools.

The goals of floorplanning :

-> Arrange the block on a chip

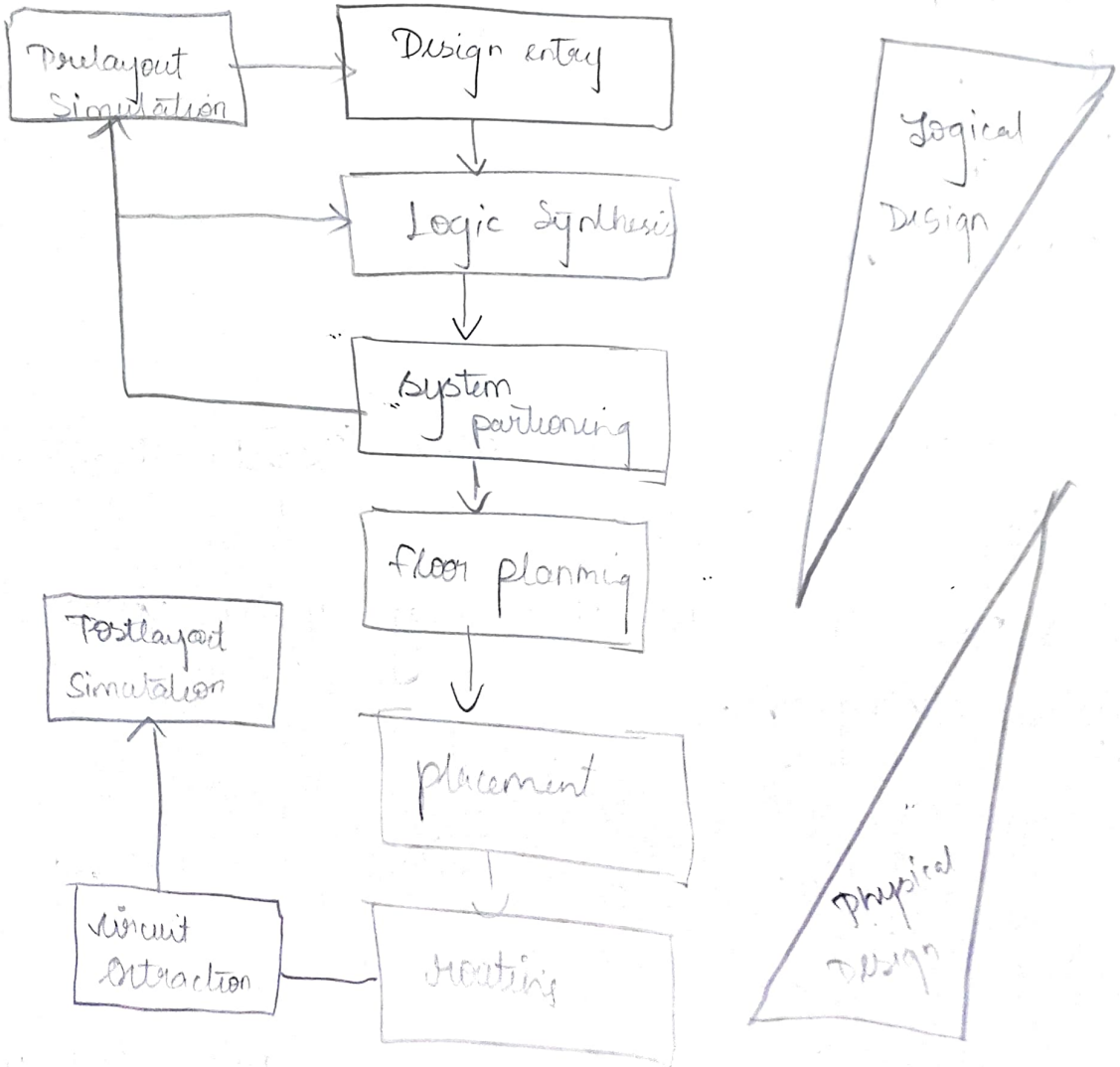
-> Decide the location of the I/O pads

-> Decide the location of the power

-> distribution

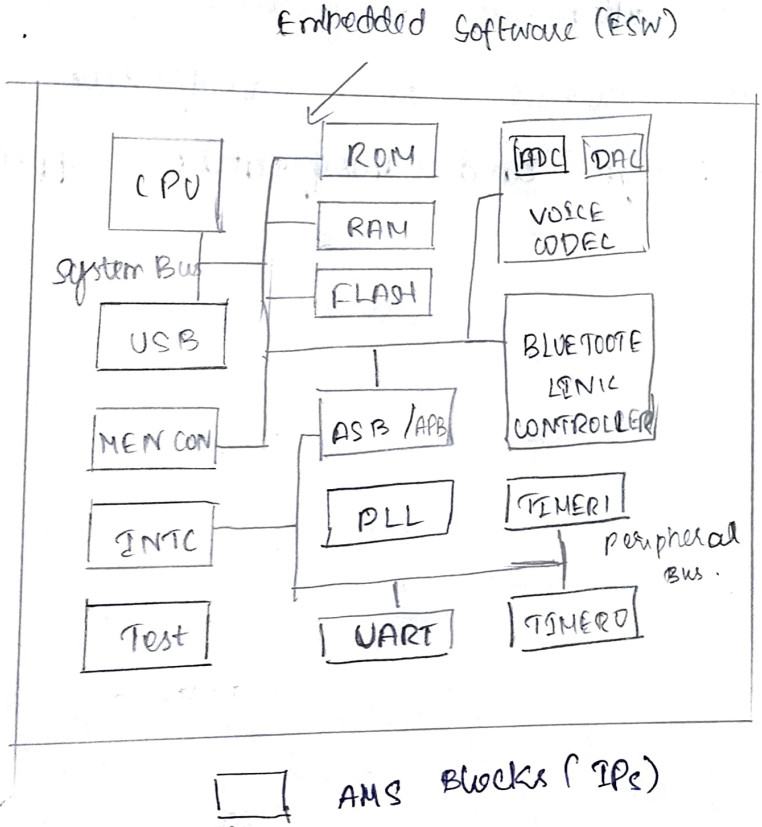
-> Decide the location and type of clock distribution .

Schemmatic Diagram of ASIC Design Flow .



Microchip Design process and issues in Test and verification of complex chips. Embedded cores and SOCs.

⇒ An SOC includes programmable elements (control processors and digital signal processors (DSP), hardware elements (digital and analog / mixed signal (AMS) blocks), software elements, complex bus architectures, clock and power distribution, test structures, and buses.



Block diagram of SOC

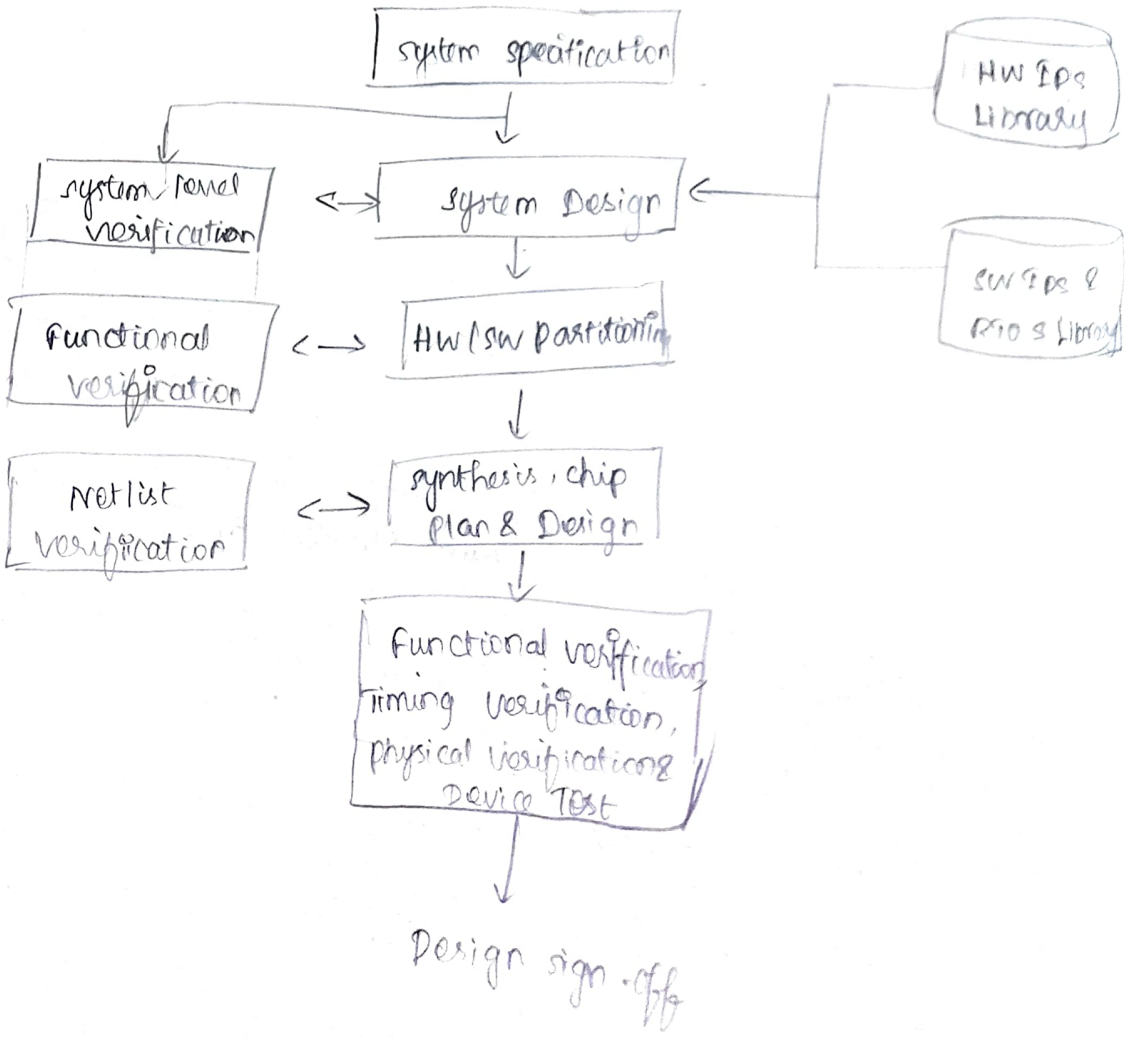
⇒ This represents challenges over traditional design methodologies where different design disciplines

(digital, AMS, embedded software (ESW)) could be designed in isolation with methodologies and tools specific to each discipline.

⇒ The tools must also deal with the added complexity of SOC devices, not only due to the increased gate counts but also the complex structures and algorithms implemented on these devices.

⇒ These include top-down design and verification, bottom-up verification, platform based verification and system interface-driven verification.

Top-Down Design and verification approach.



Scan Design :

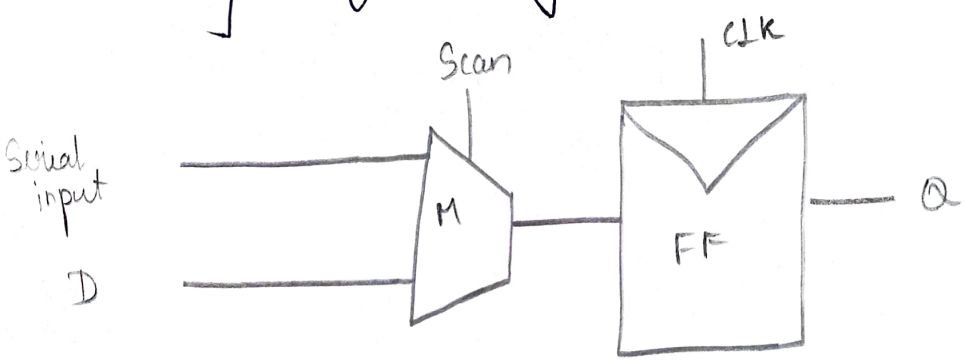
Serial Scan :

In Scan Design, the registers operate in one of two modes.

* Normal mode -> they behave as expected
* Scan mode -> they are connected to form a giant register called chains spanning the whole chip.

Applying N clock pulses in Scan mode, all N bits of state in the system can be shifted in the single mode.

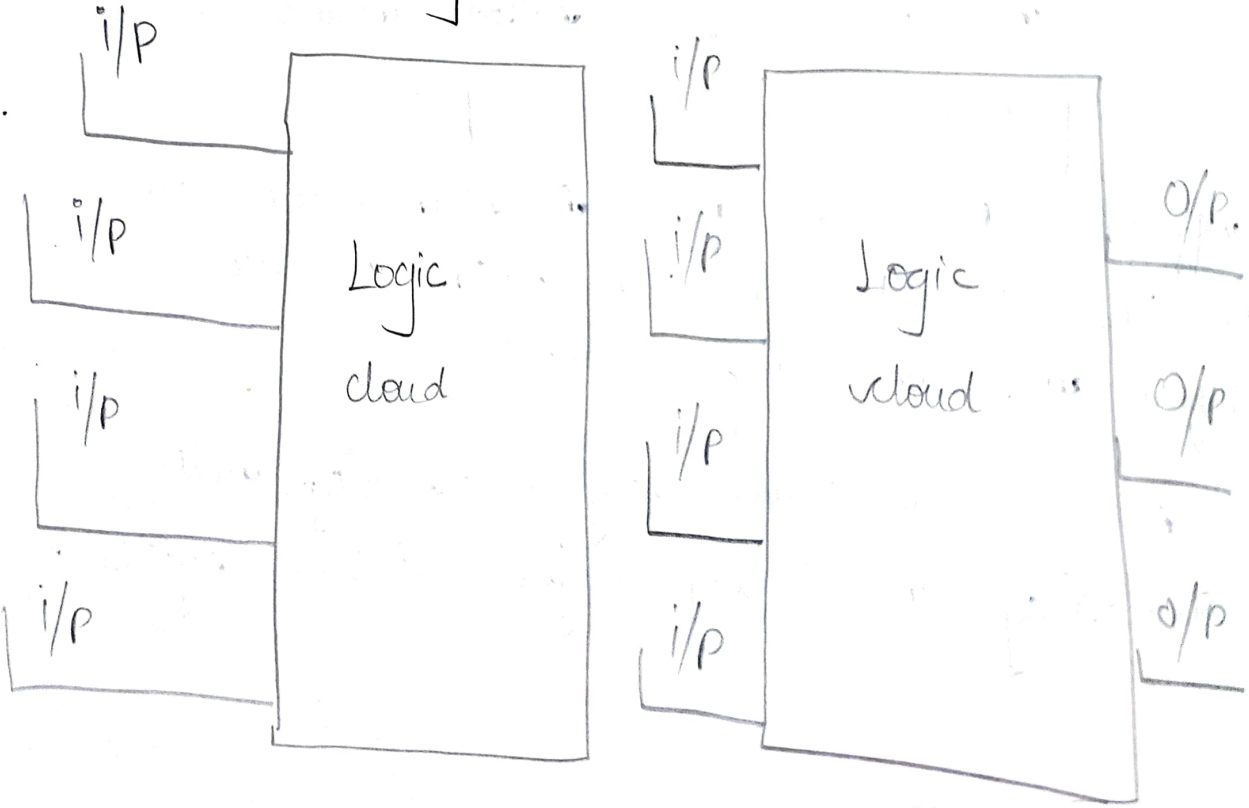
Scan mode gives easy observability and controllability of every register in the system.



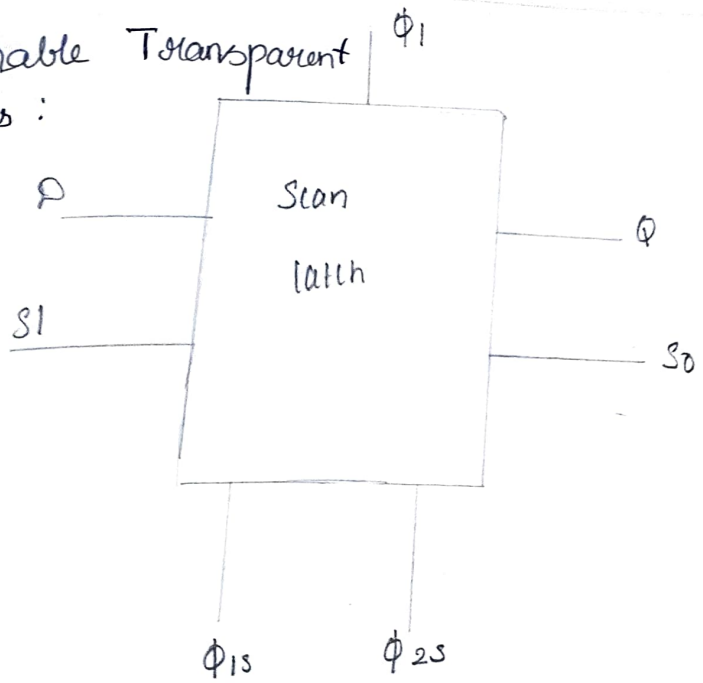
Serial Scanner.

clk	Scan	D	SI	Q	Comment
↑	1	X	0	0	Q is same
↑	1	X	1	1	DFF
↑	0	0	X	0	Q
↑	0	1	X	1	DFF

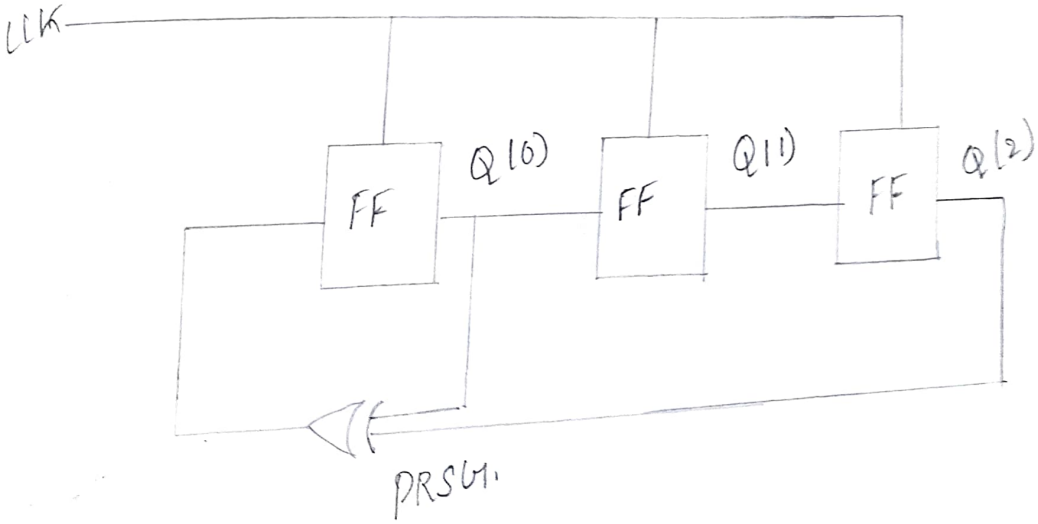
Scan Based Testing :



Scannable Transparent latches :



Built in Self Test



Built - in Logic Block observation :